

Project Name : A14HV02

Platform : Sandy Bridge(PROCESSOR)+Couagr Poinrt(PCH)

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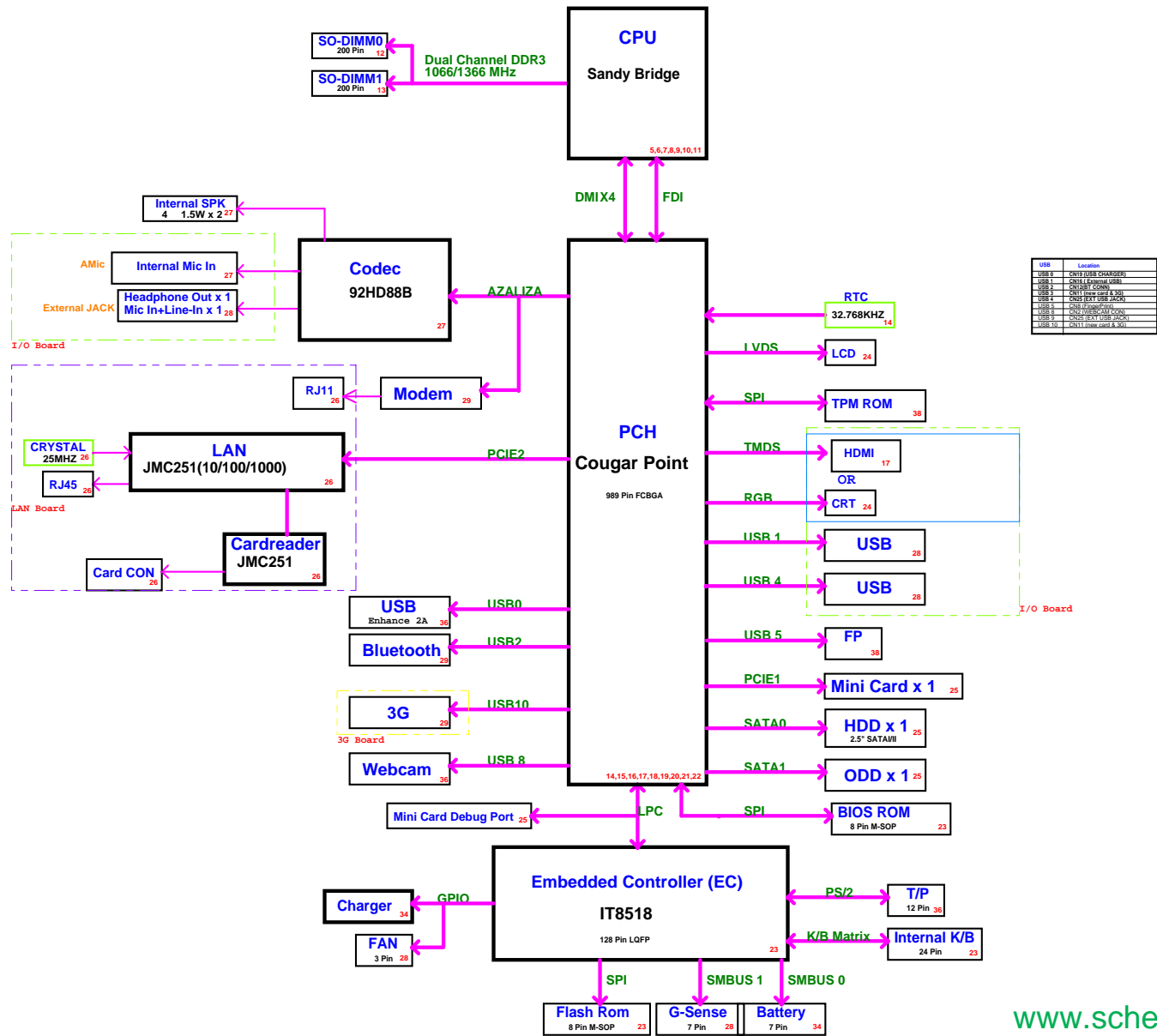
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

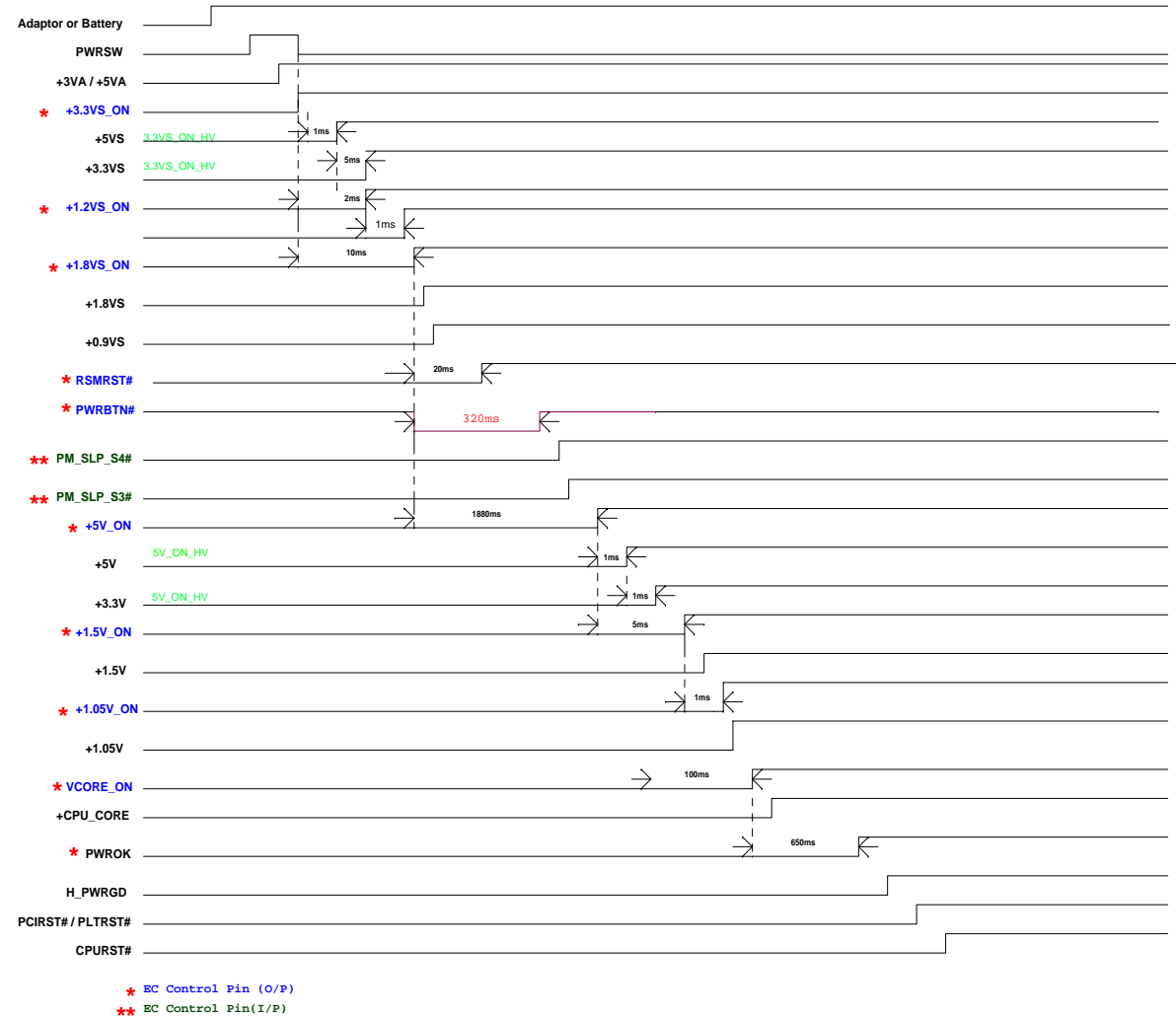
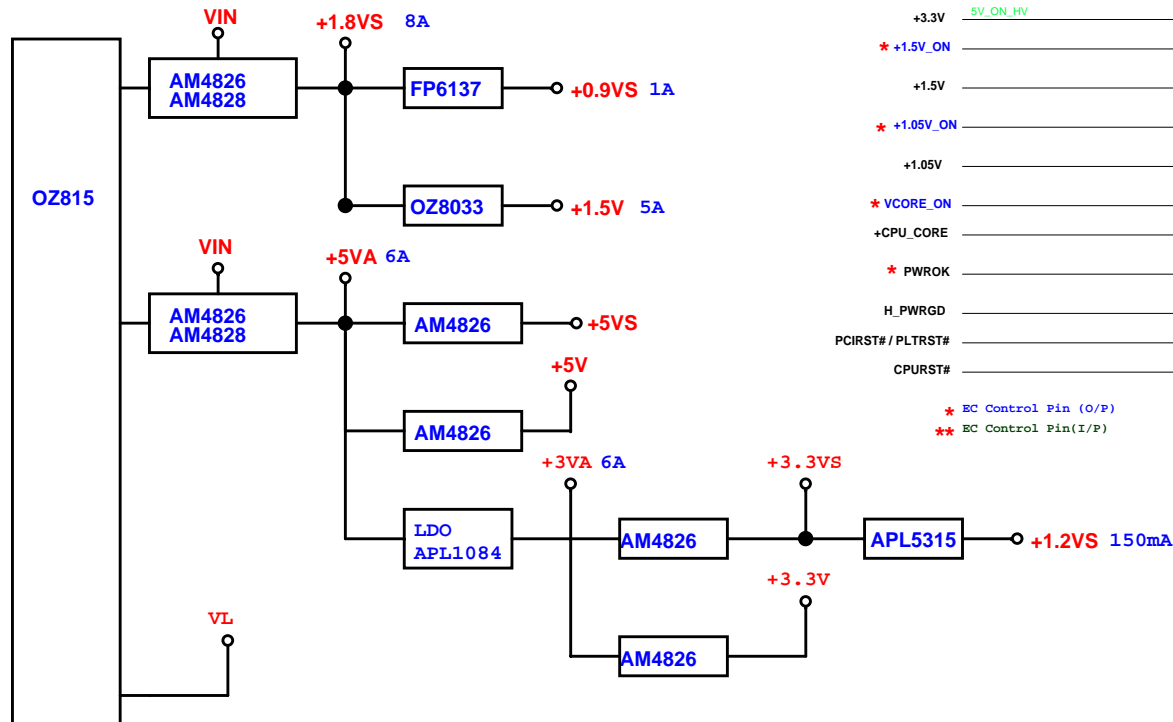
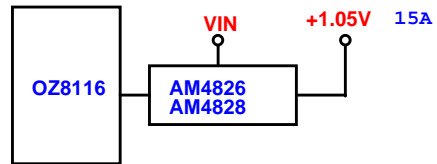
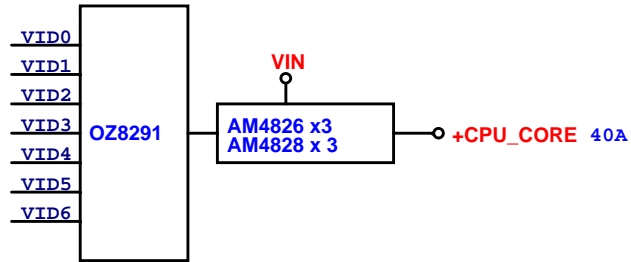
SYSTEM BLOCK DIAGRAM



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# POWER BLOCK DIAGRAM

# System Poewr On Sequence



ICH9M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQ#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	<b>N.C</b> (TACH3)
GPIO8	<b>N.C</b>
GPIO9	<b>N.C</b> (WOL_EN)
GPIO10	<b>N.C</b> (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	<b>N.C</b> (GLAN_DOCK#)
GPIO14	<b>N.C</b> (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	<b>N.C</b> (TACH0)
GPIO18	<b>N.C</b>
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	<b>N.C</b> (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	<b>N.C</b> (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8518 GPIO		Default Pull/Mode
GPA0	PID_3_RF_LED_ON#	UP / GPI
GPA1	BATT_VA_OFF#	UP / GPI
GPA2	BTLL_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	+1.05V_ON	UP / GPI
GPA5	SENBAT_V	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	3G_PWR#	Dn / GPI
GPB3	SMBCLK	/ GPI
GPB4	SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Funcl
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMB_CLK_EC	/ GPI
GPC2	SMB_DAT_EC	/ GPI
GPC3	<b>PID_0_CHG_B_LED</b>	Dn / GPI
GPC4	PWRBTN3#	Dn / GPI
GPC5	PANEL_DETECT_2	Dn / GPI
GPC6	VCCSA_ON	Dn / GPI
GPC7	+1.5VS_ON	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Funcl
GPD3	<b>PM_SUS_STAT#</b>	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	Fastcharge_EN	UP / GPI
GPD6	<b>+5V_ON</b>	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	PWR_USB_LED	Dn / GPI
GPE2	ALL_SYS_PGD	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPI
GPE6	WLAN_ON	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	PCH_BL_EN	UP / GPI
GPF1	<b>+1.8V_ON</b>	UP / GPI
GPF2	<b>BT_ON</b>	UP / GPI
GPF3	<b>N.C</b>	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	<b>EC PECl</b>	UP / GPI
GPF7	<b>CHG_HI VOLT#</b>	UP / GPI
GPG0	PWRBTN2#	Dn/GPO/TM
GPG1	+3.3VS_ON	Dn/GPO/ID7
GPG2	<b>EC PORST</b>	
GPG6	WEBCAN_ON	Dn / GPI
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PID_1_CHG_R_LED	Dn/GPI/ID1
GPH2	PID_2_PWR_LED	Dn/GPI/ID2
GPH3	EC_HSCS0#	Dn/GPI/ID3
GPH4	EC_HSCK	Dn/GPI/ID4
GPH5	EC_HMISO	Dn/GPI/ID5
GPH6	EC_HMOSI	Dn/GPI/ID6

ITE8518 GPIO		Default Pull/Mode
GPI0	<b>CRT_DETECT</b>	/GPI/ADC
GPI1	PANEL_DETECT	/GPI/ADC
GPI2	PLATFORM_ID	/GPI/ADC
GPI3	<b>CPPE#</b>	/GPI/ADC
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTOR_1	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_ON	/GPI/DAC
GPJ1	EC_PROCHOT	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	PWR_USB#	/GPI/DAC

Penryn CPU				
	CPU CORE(V)	ICC(A)	W	TEMP ( )
IMVP-6+	1.05	44.0	36	

Cantiga			
VCC	ICC(mA)	W	TEMP ( )
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

ICH9M			
VCC	ICC(mA)	mW	TEMP ( )
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

ITE8500			
VCC	ICC(mA)	mW	TEMP ( )
+3.3V	100	330	70

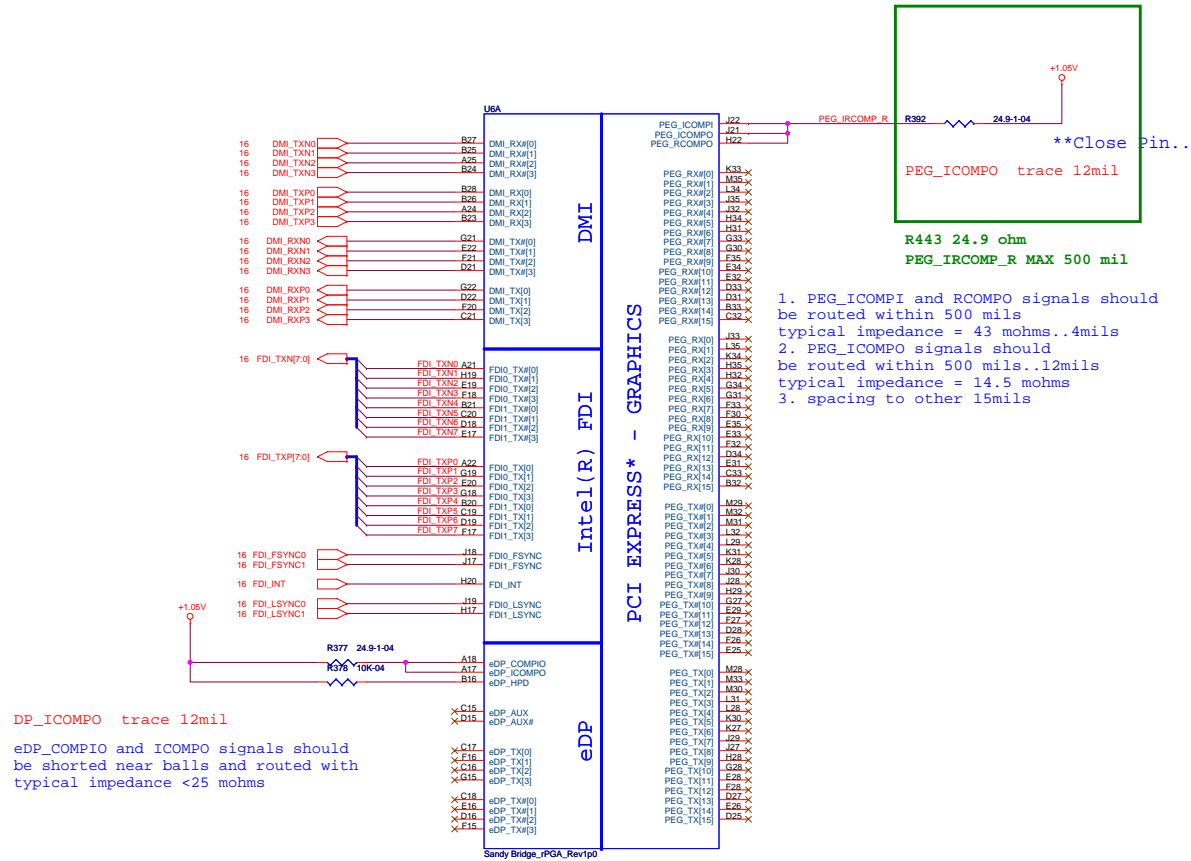
CLOCK GENERATOR			
VCC	ICC(mA)	mW	TEMP ( )
+3.3V	1000	3300	70

IDT92HD81			
VCC	ICC(mA)	mW	TEMP ( )
+3.3V(DVDD)	200	660	70
+5V(AVDD)	1000	5000	

ADM1032			
VCC	ICC	mW	TEMP ( )
+3.3V	170uA	0.56	150

JMC261			
VCC	ICC(mA)	mW	TEMP ( )
+3.3VS	300	990	70
+1.2VS	150	180	

## SANDYBRIDGE PROCESSOR(DMI,PEG,FDI)

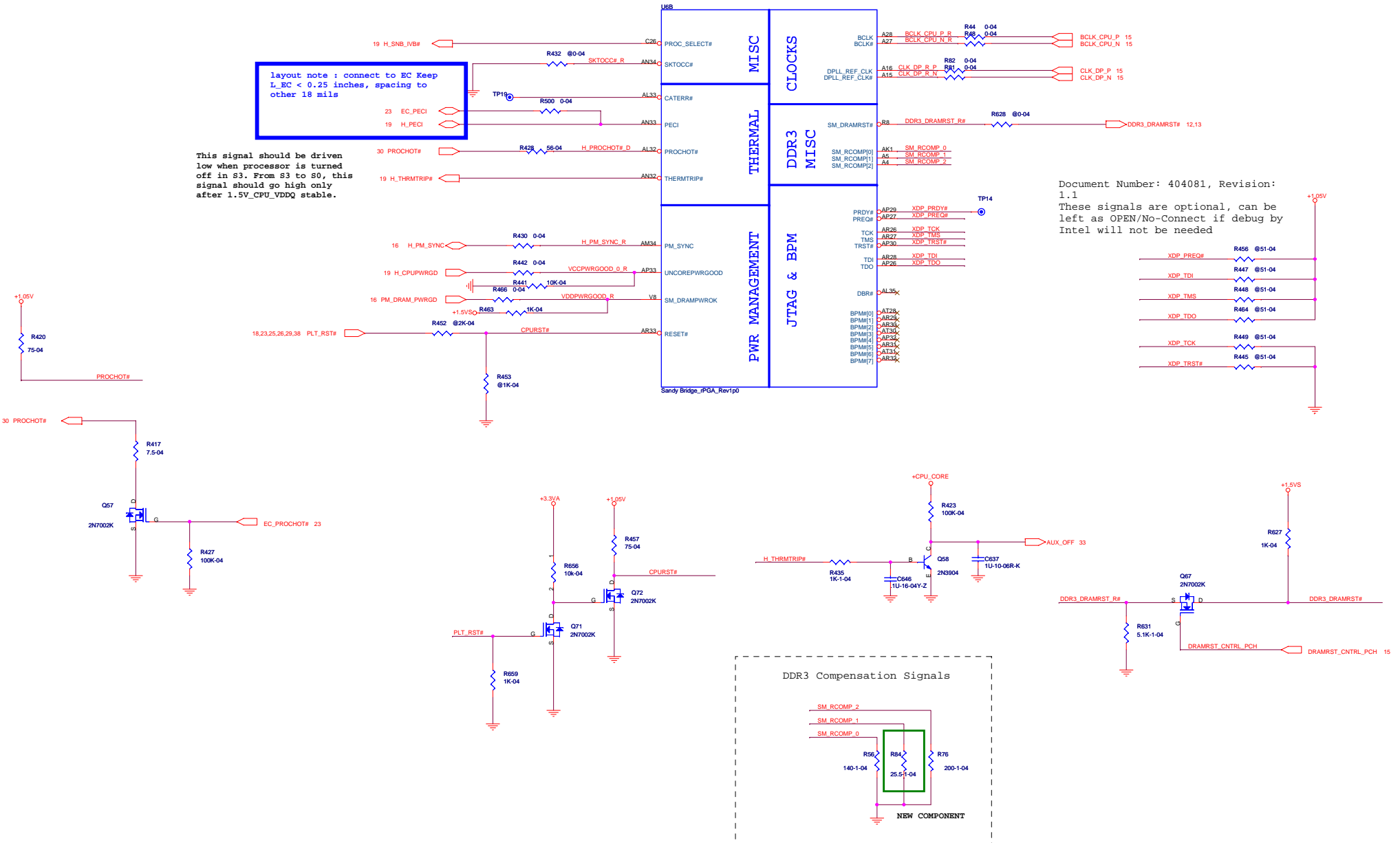


# SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)

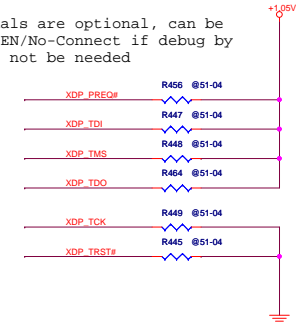
This pin is for compability with future platforms. A pull up resistor to VCPLL is required if connected to the DF\_TVS strap on the PCH.

layout note : connect to EC Keep  
L\_EC < 0.25 inches, spacing to  
other 18 mils

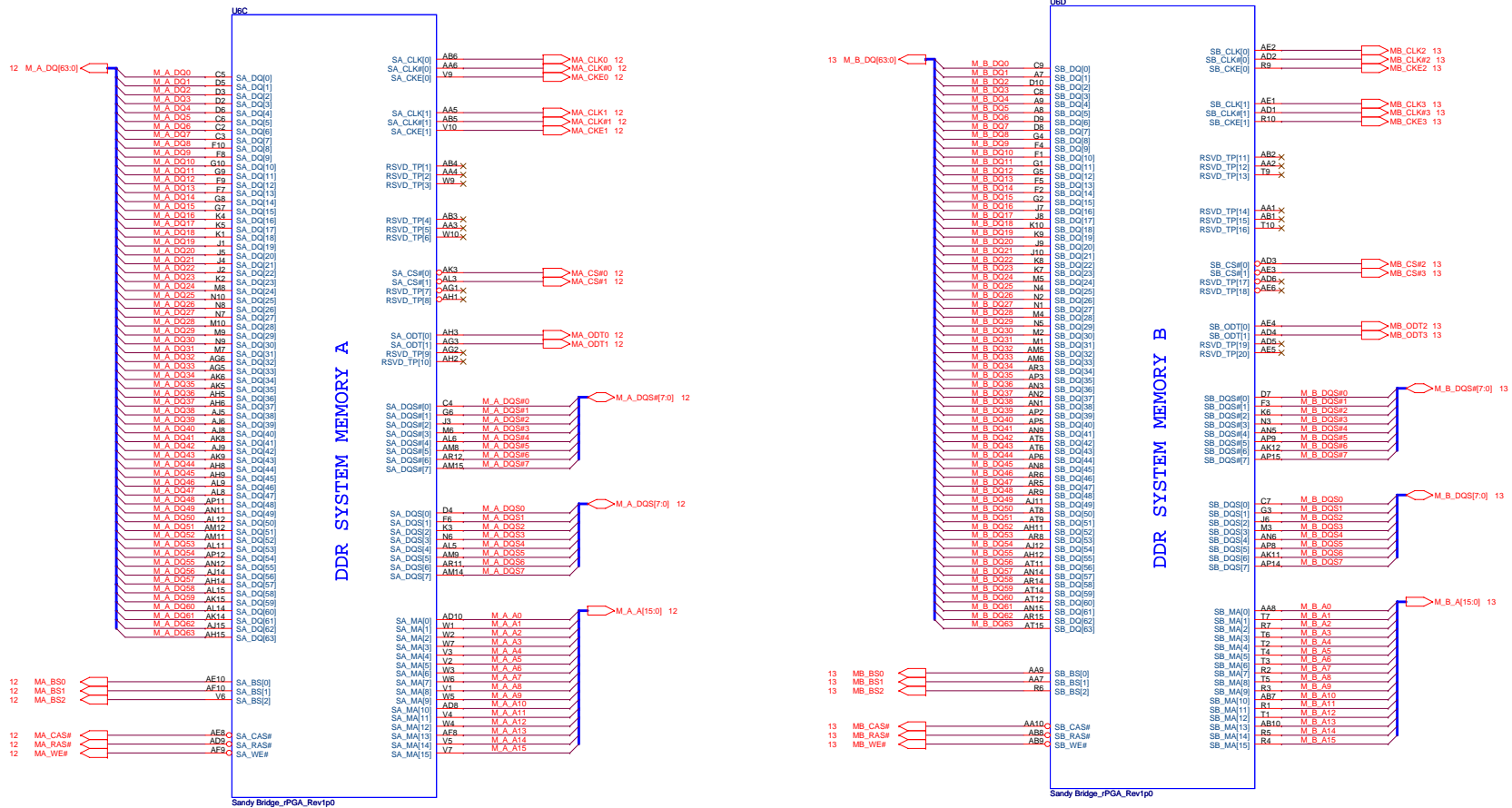
This signal should be driven  
low when processor is turned  
off in S3. From S3 to S0, this  
signal should go high only  
after 1.5V\_CPU\_VDDQ stable.



Document Number: 404081, Revision:  
1.1  
These signals are optional, can be  
left as OPEN/No-Connect if debug by  
Intel will not be needed



# SANDYBRIDGE PROCESSOR (DDR3)

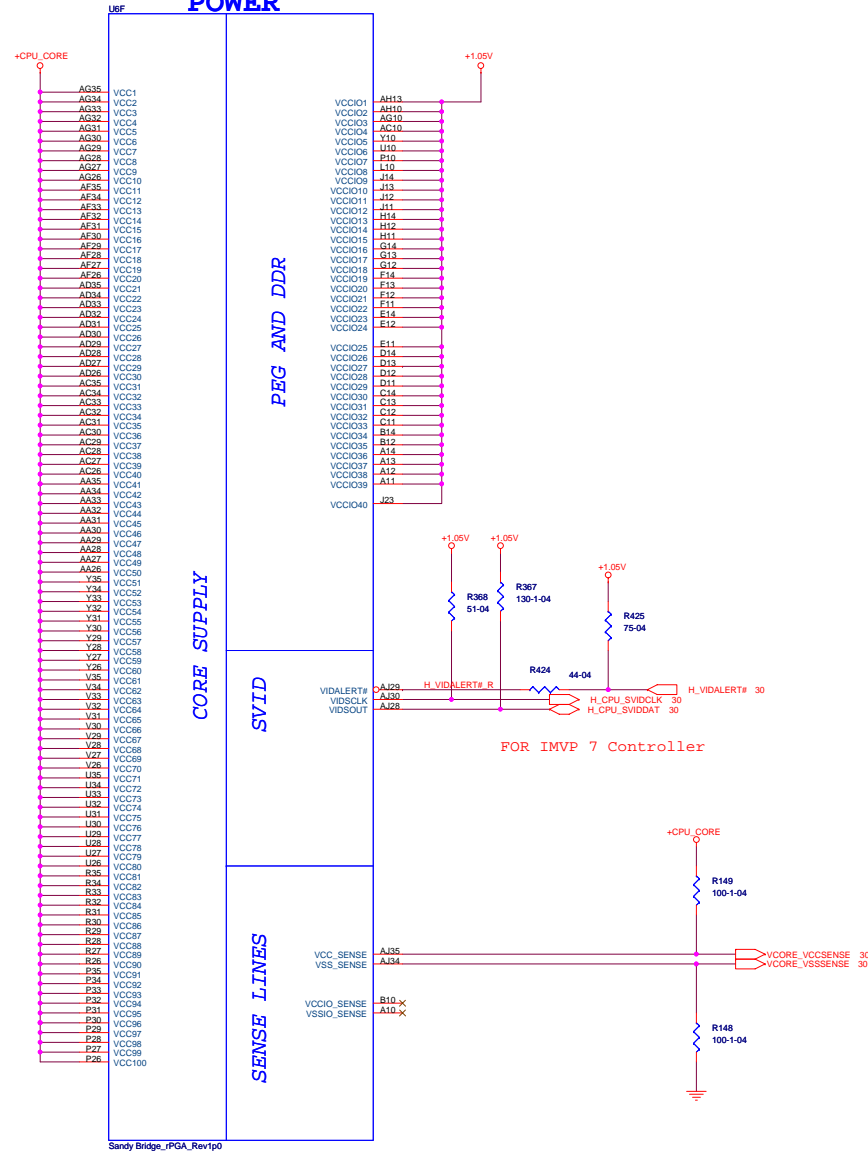


Sandy Bridge\_PGA\_Rev1p0

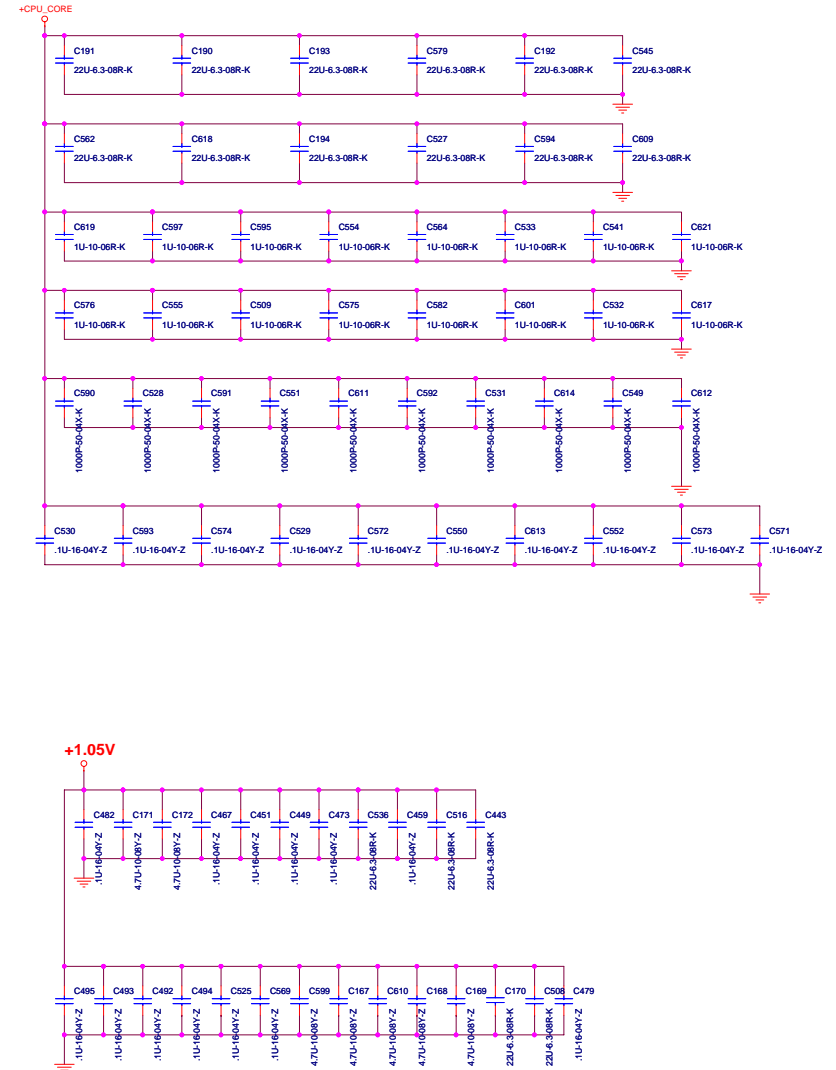
Sandy Bridge\_PGA\_Rev1p0

# SANDYBRIDGE PROCESSOR (POWER)

## POWER

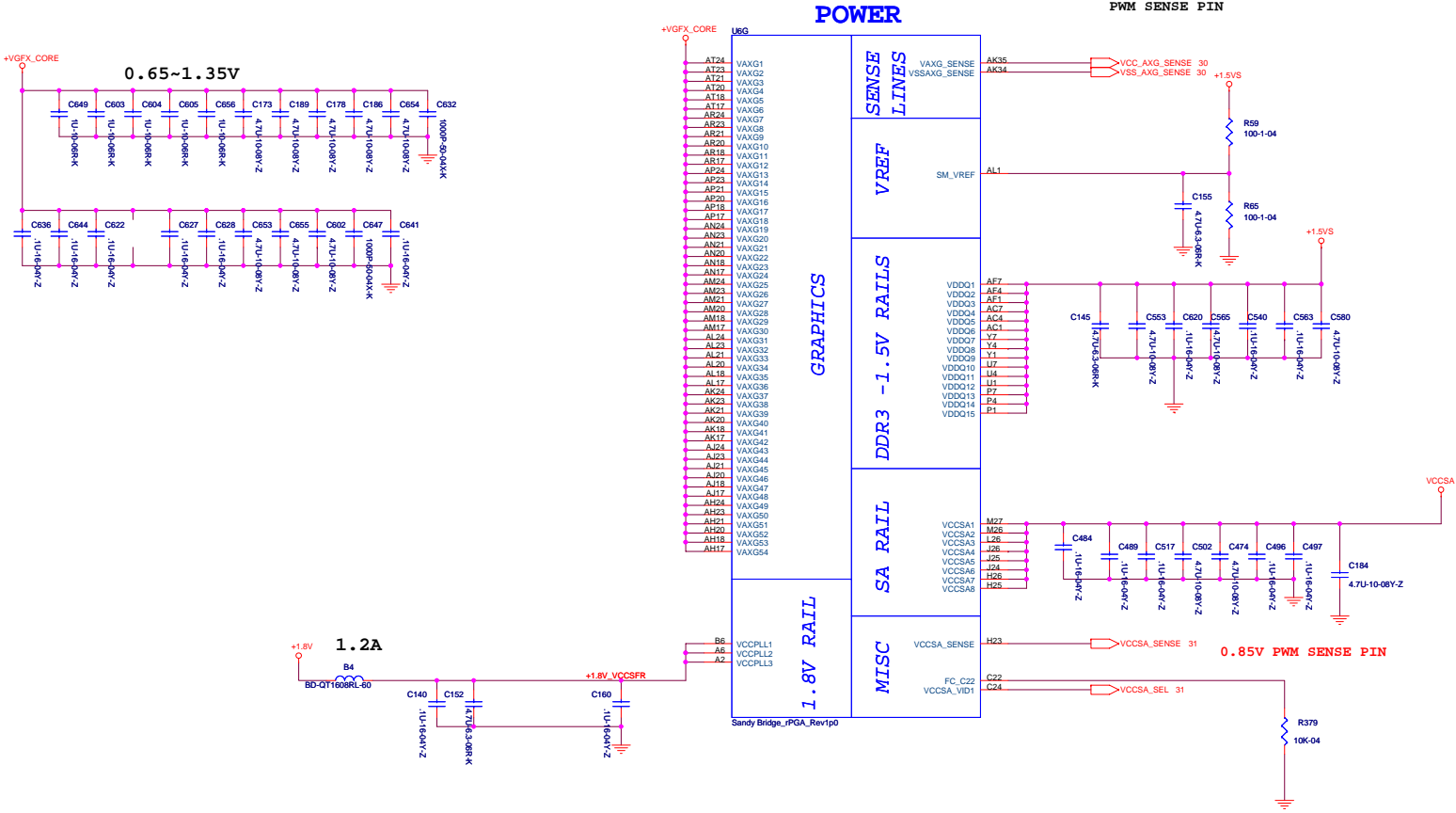


## +CPU\_Core Decoupling

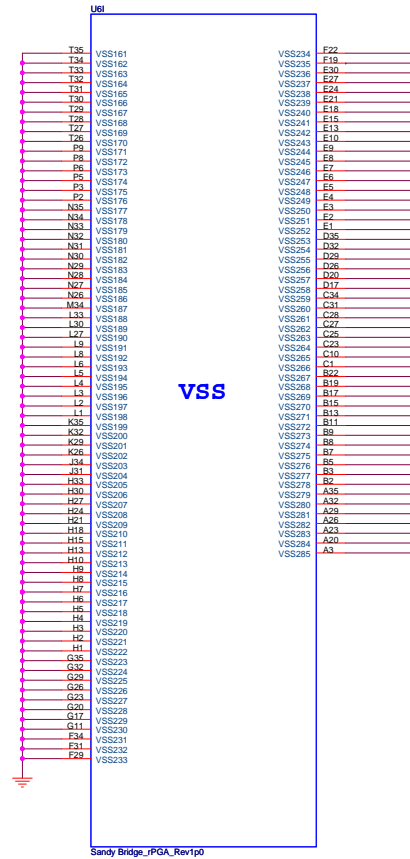
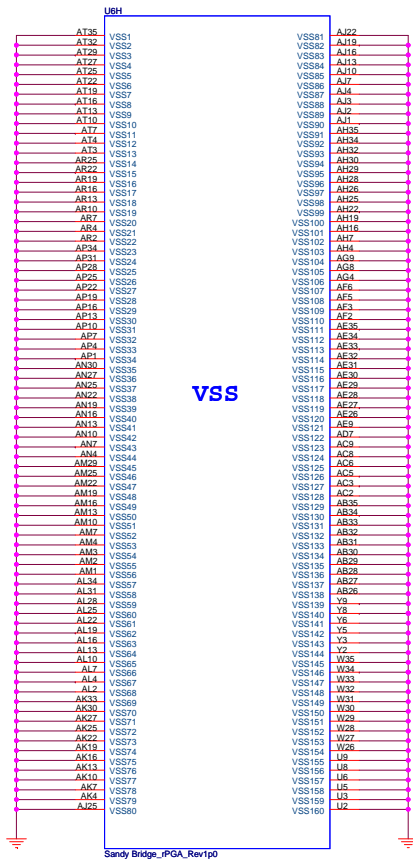




SANDYBRIDGE PROCESSOR (POWER)



# SANDYBRIDGE PROCESSOR (VSS)



# SANDYBRIDGE PROCESSOR (RESERVED)

PCIE Port Bifurcation Straps

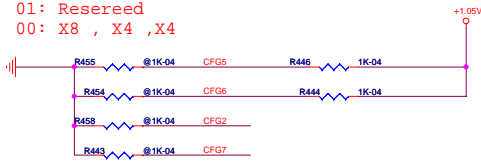
CFG[6:5]

11: (Default) X16

10: X8 , X8

01: Resereed

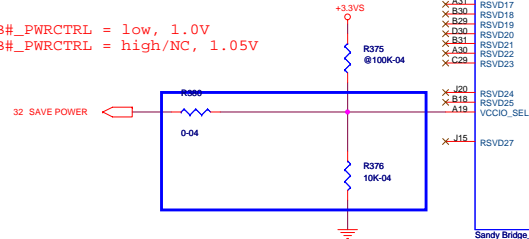
00: X8 , X4 ,X4



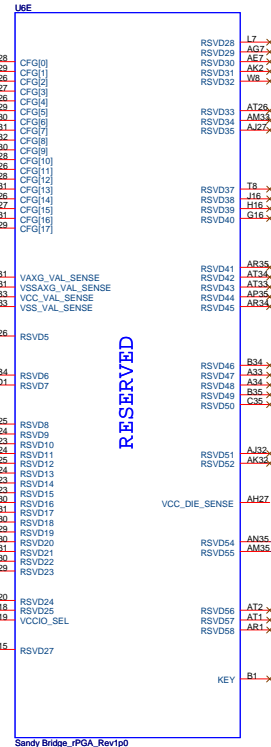
On CRB

H\_SNB\_IVB#\_PWRCTRL = low, 1.0V

H\_SNB\_IVB#\_PWRCTRL = high/NC, 1.05V

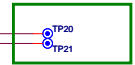


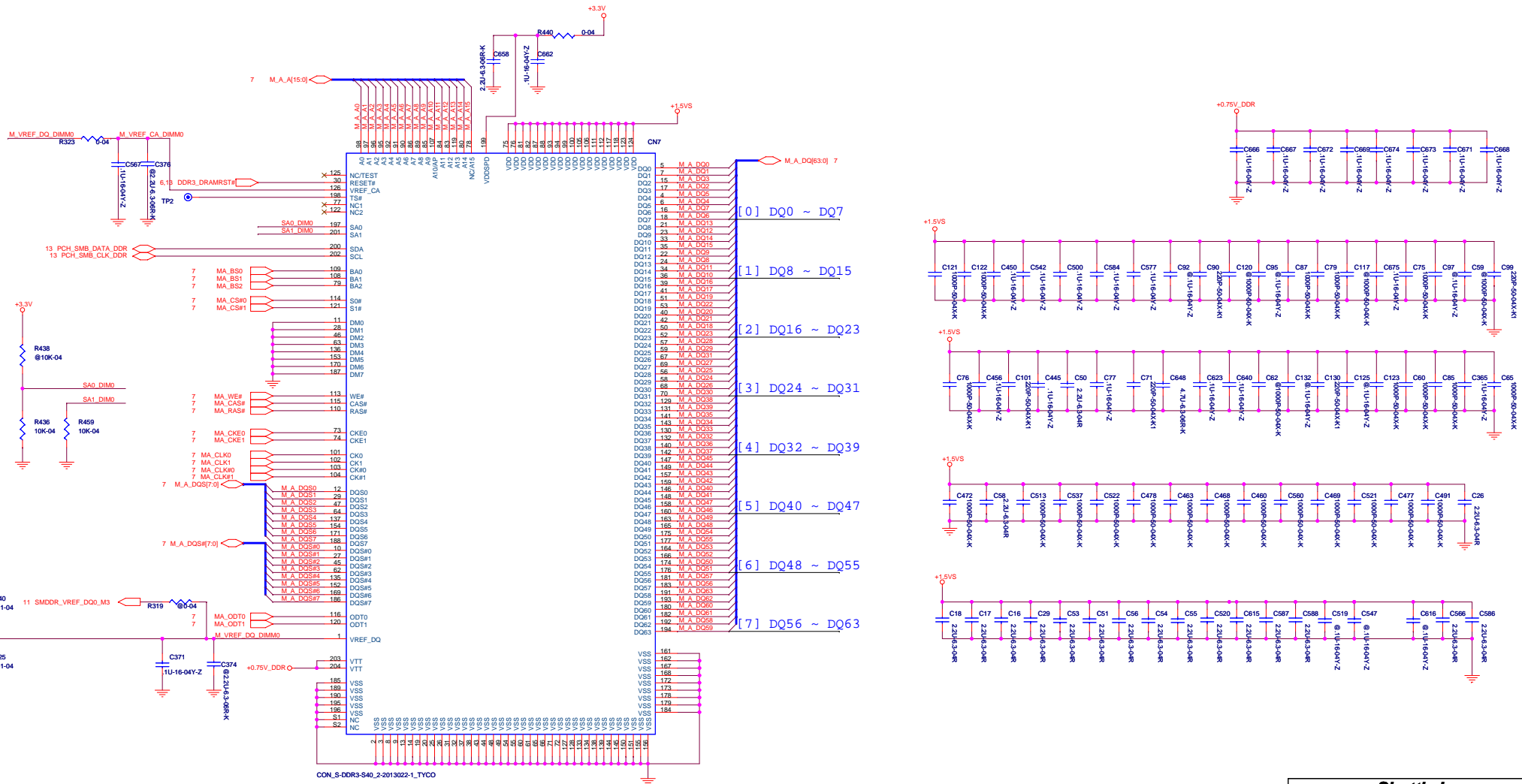
MB6:ADD 0R FOR VCCSA SENSOR



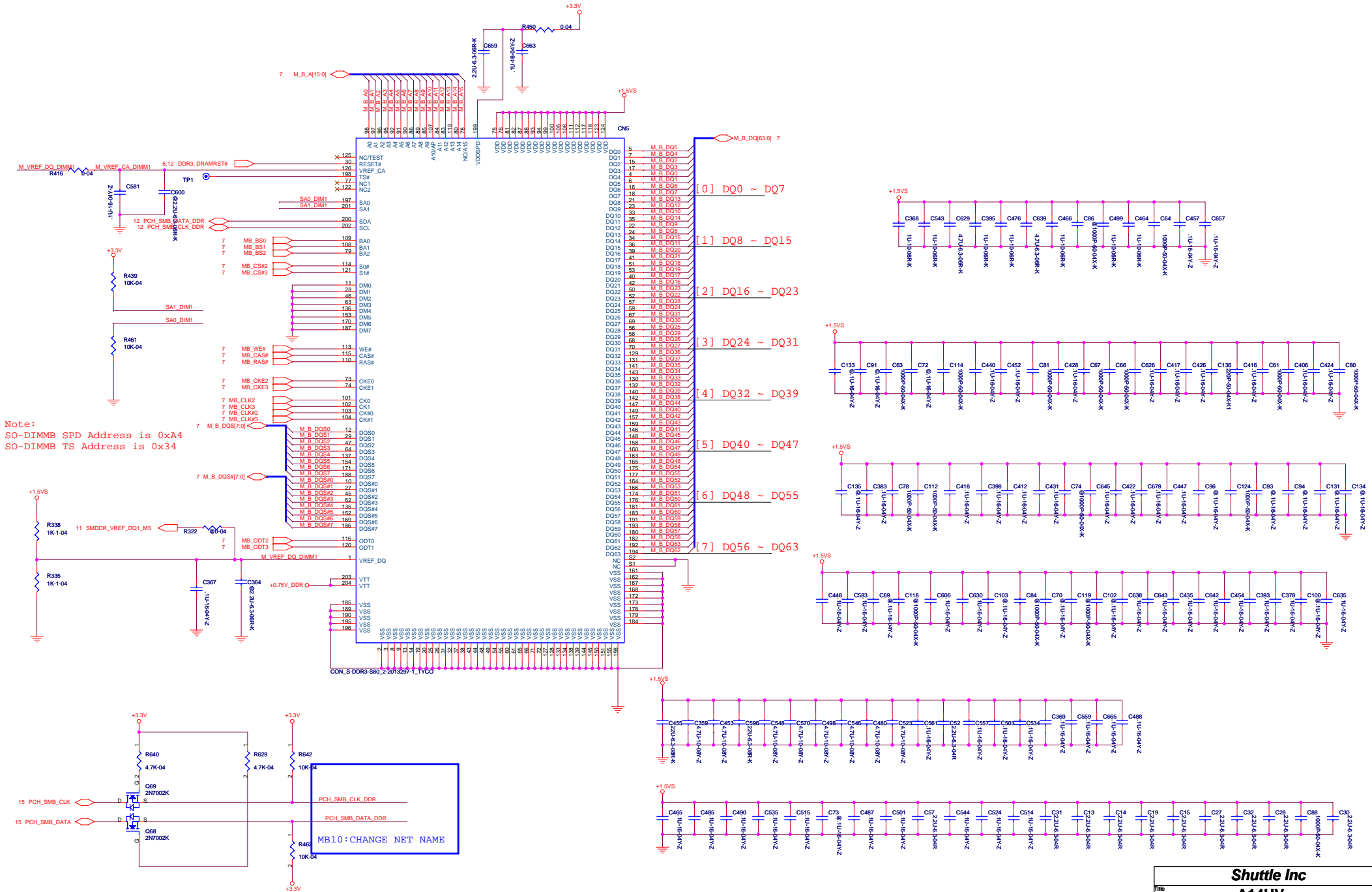
RESERVED

INTEL DEBUG CARD CLOCK

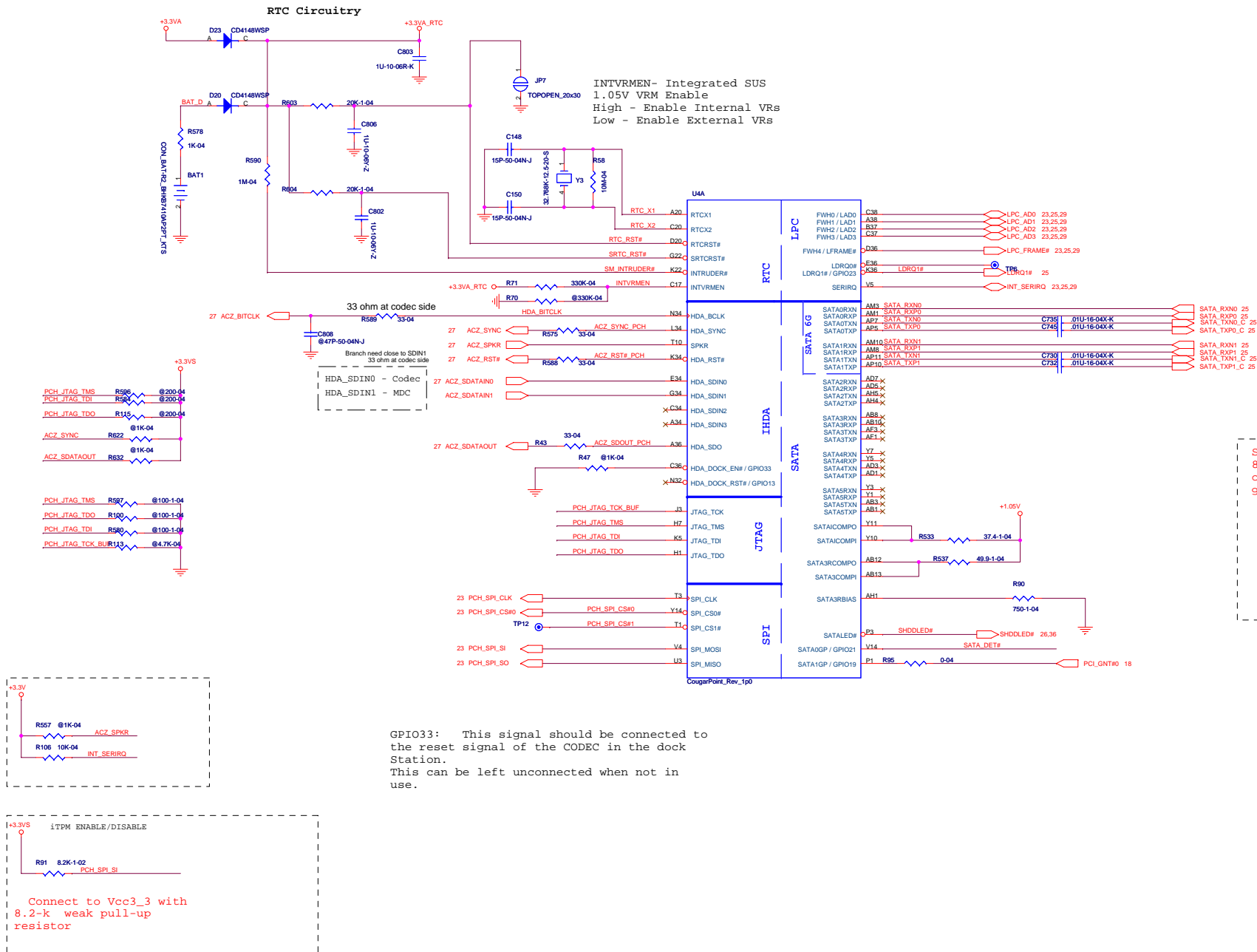




Note:  
SO-DIMMB SPD Address is 0x44  
SO-DIMMB TS Address is 0x34

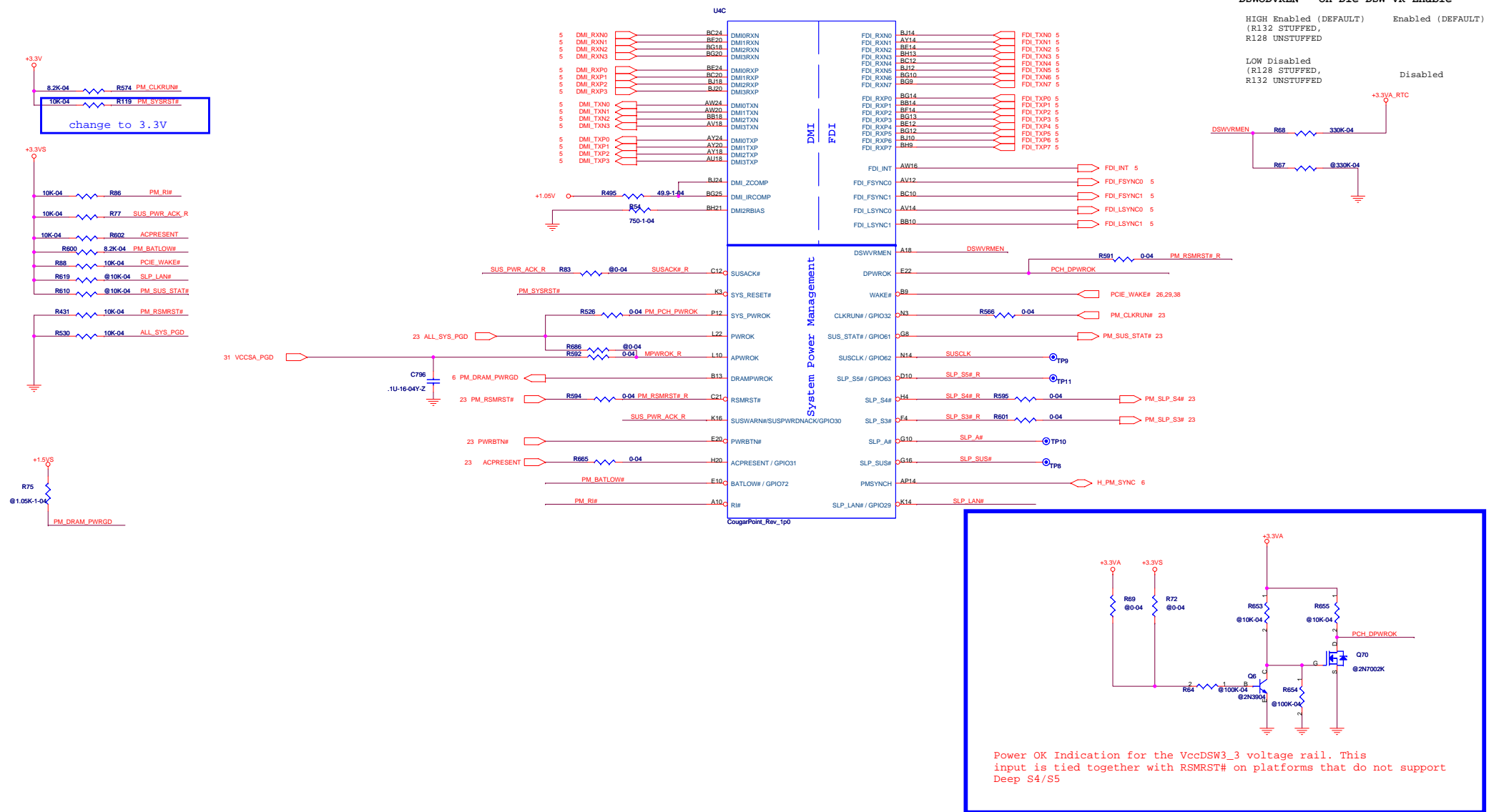


## Cougar Point Chipset (RTC,LPC,SATA,HDA,SPI,JTAG)



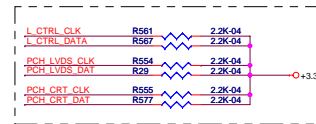
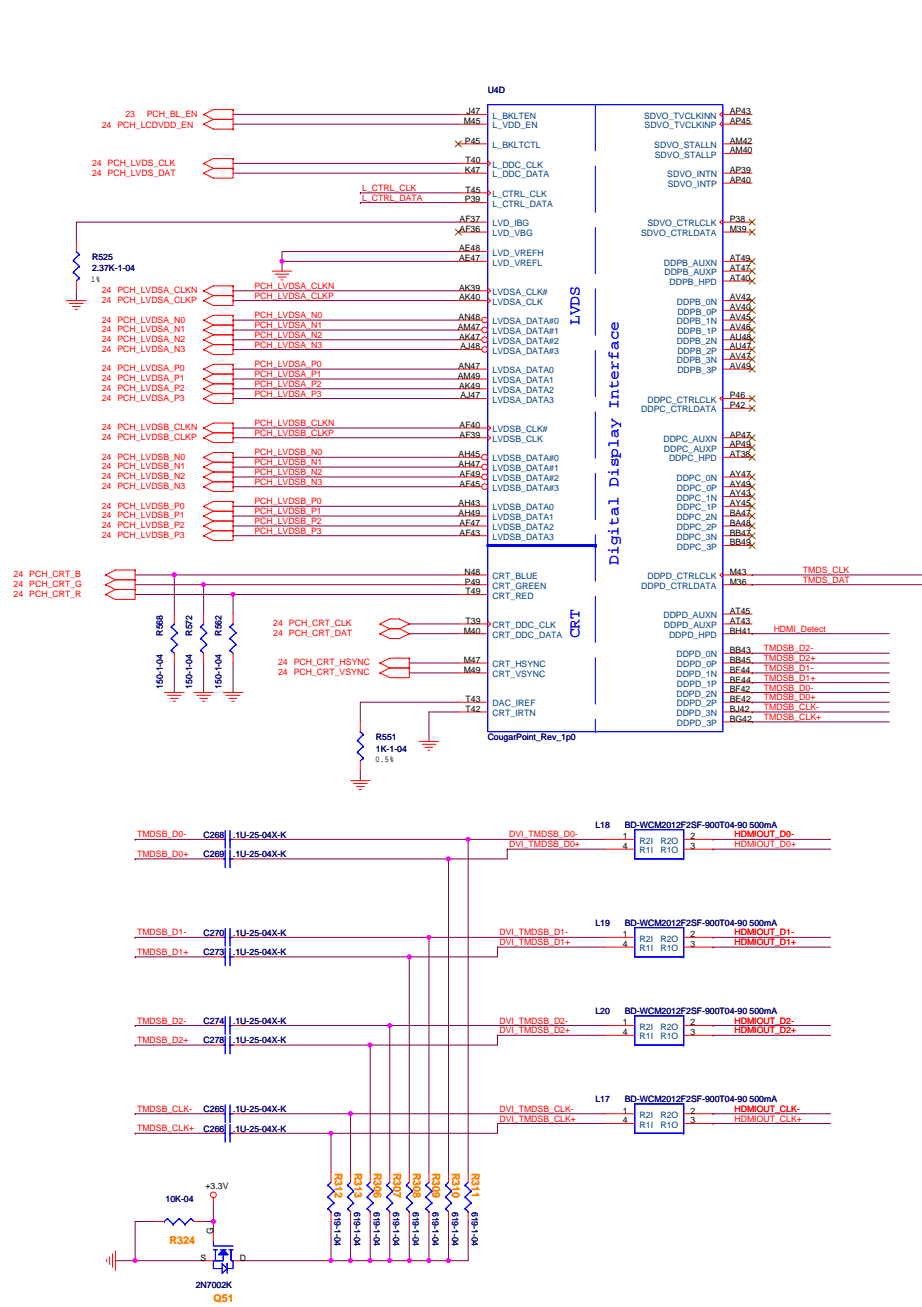
[illegible][illegible][illegible][illegible]

# Cougar Point Chipset (DMI,FDI)



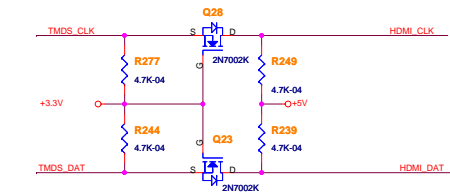


# Cougar Point Chipset (LVDS,CRT,Digital Display)

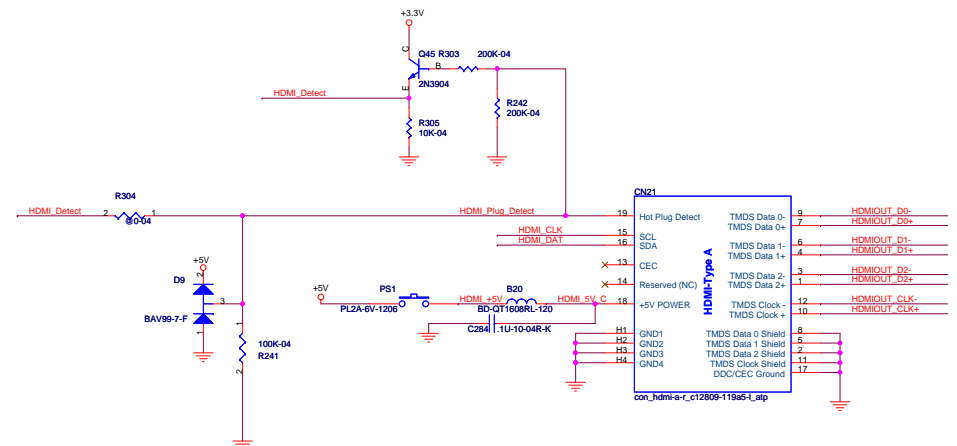


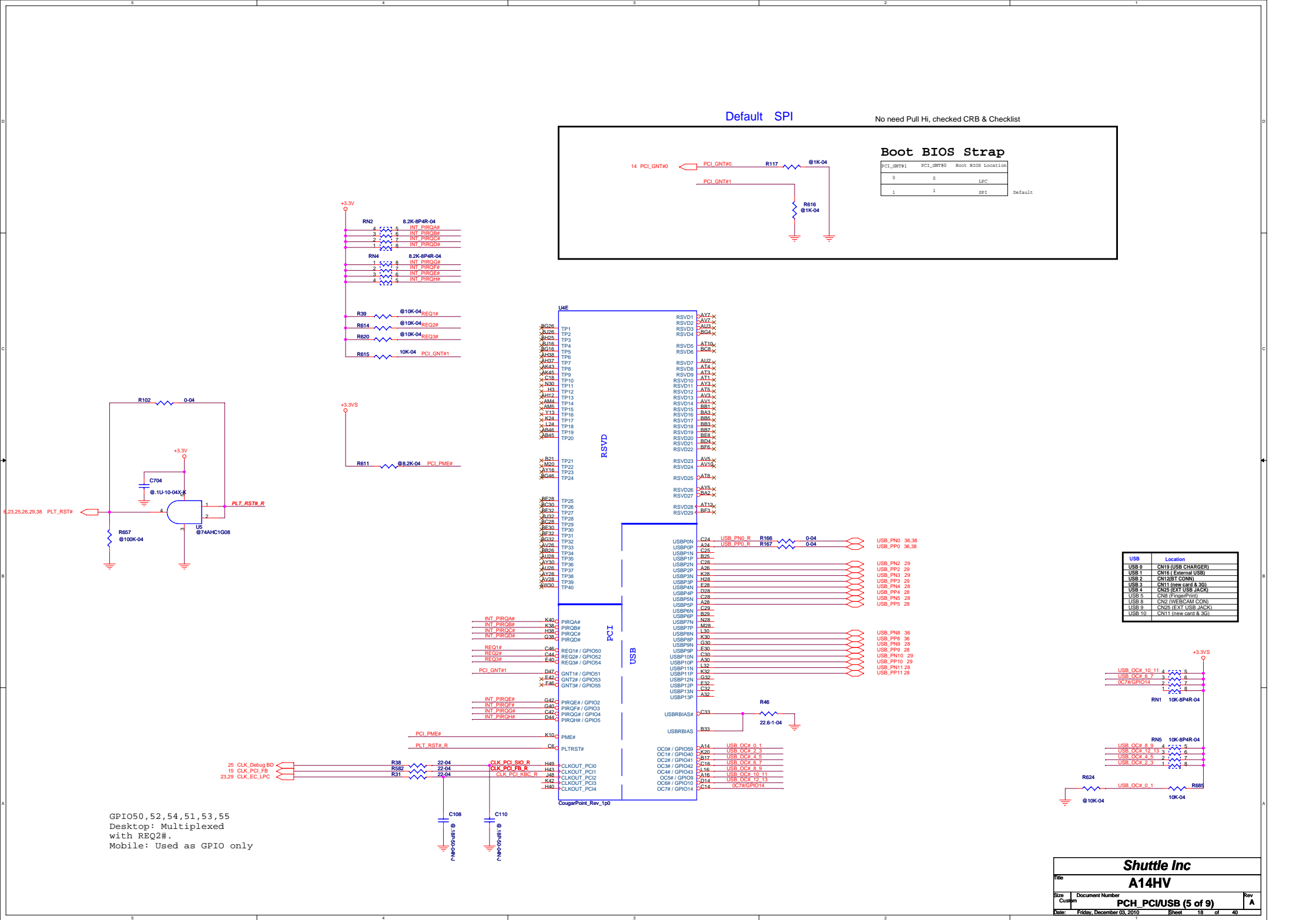
Configuration Wise Pin Mapping for DDI Ports (Sheet 1 of 2)

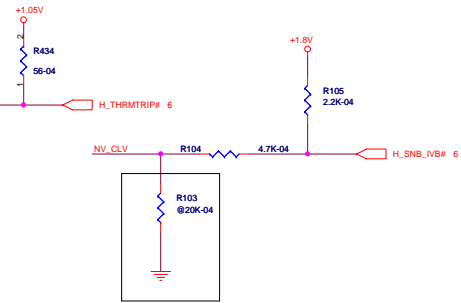
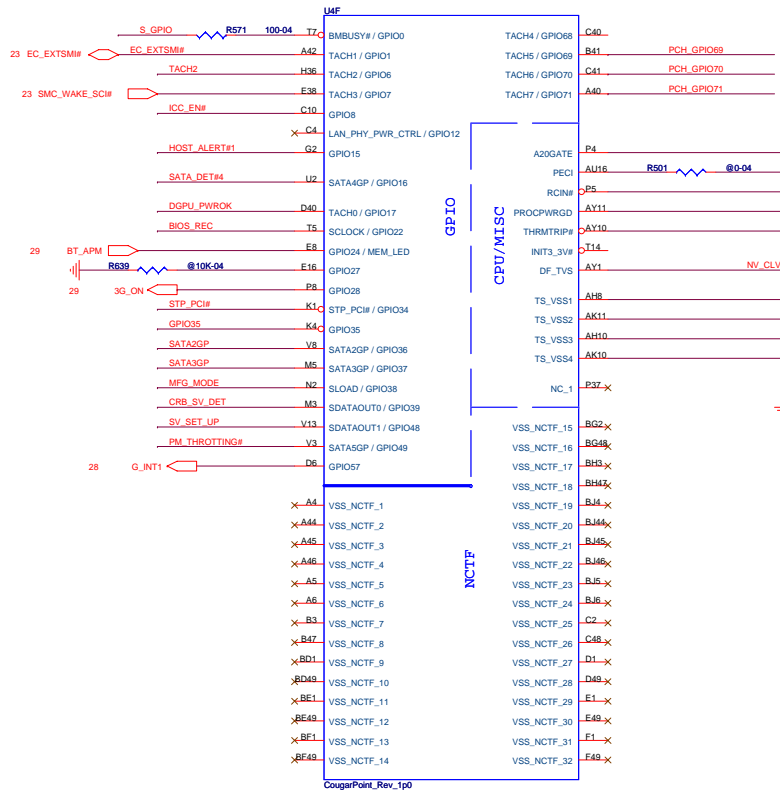
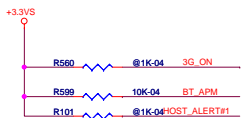
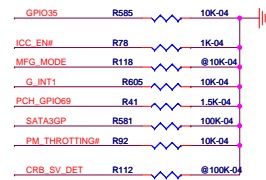
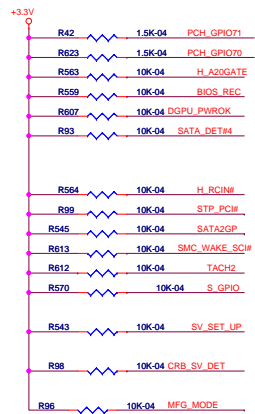
PORT	DDI PCH Pin Names	SDVO Mapping	DisplayPort <sup>1</sup> Mapping	HDMI/DVI Mapping
PORT-B	DDPB_00P	SDVO_RED	DDPB_00P	THDSB_DATA2
	DDPB_00N	SDVO_RED#	DDPB_00N	THDSB_DATA2#
	DDPB_01P	SDVO_GREEN	DDPB_01P	THDSB_DATA1
	DDPB_01N	SDVO_GREEN#	DDPB_01N	THDSB_DATA1#
	DDPB_02P	SDVO_BLUE	DDPB_02P	THDSB_DATA0
	DDPB_02N	SDVO_BLUE#	DDPB_02N	THDSB_DATA0#
	DDPB_03P	SDVO_CLK	DDPB_03P	THDSB_CLK
	DDPB_03N	SDVO_CLK#	DDPB_03N	THDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMI10_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI10_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI10_CTRLDATA

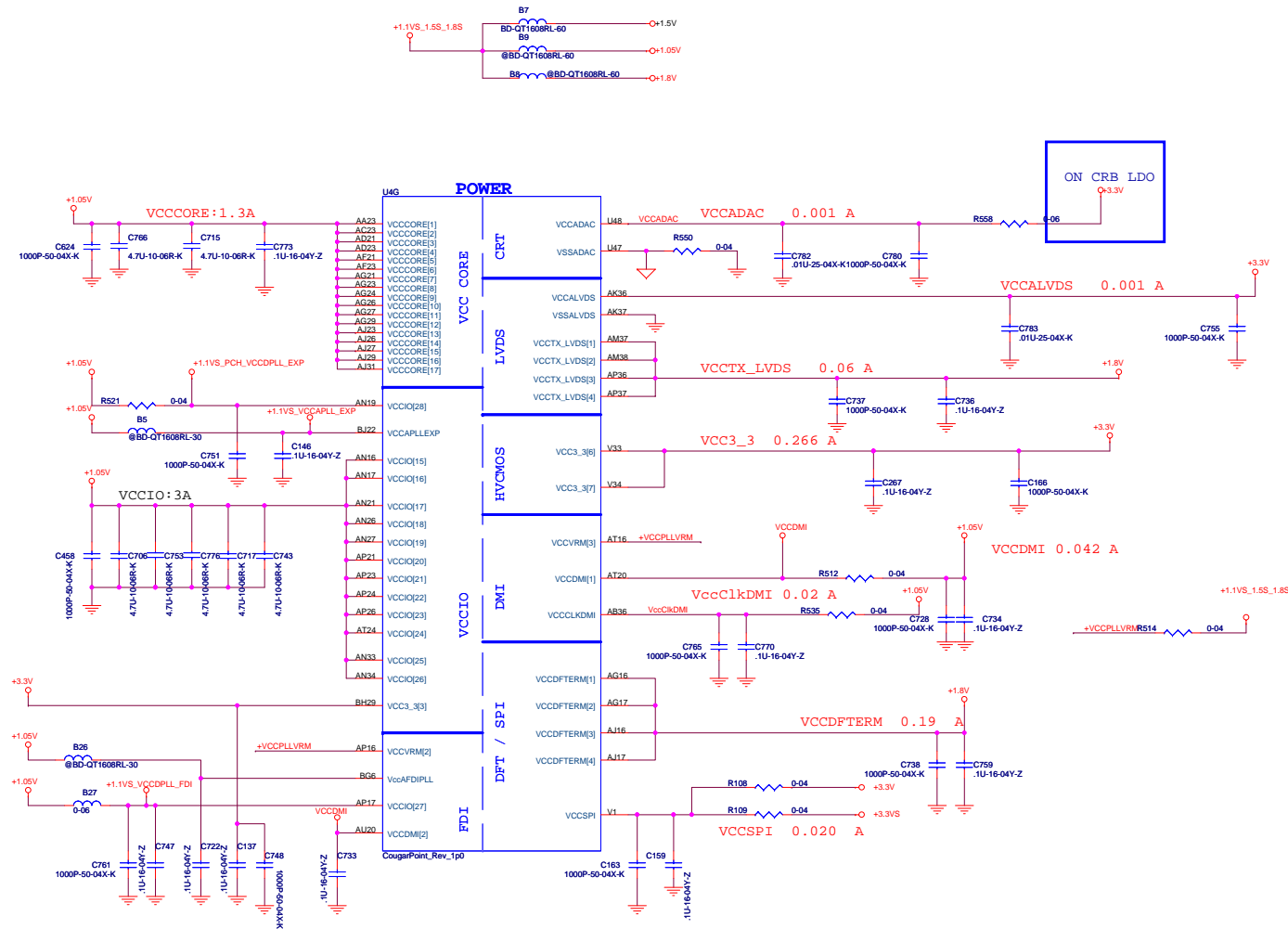


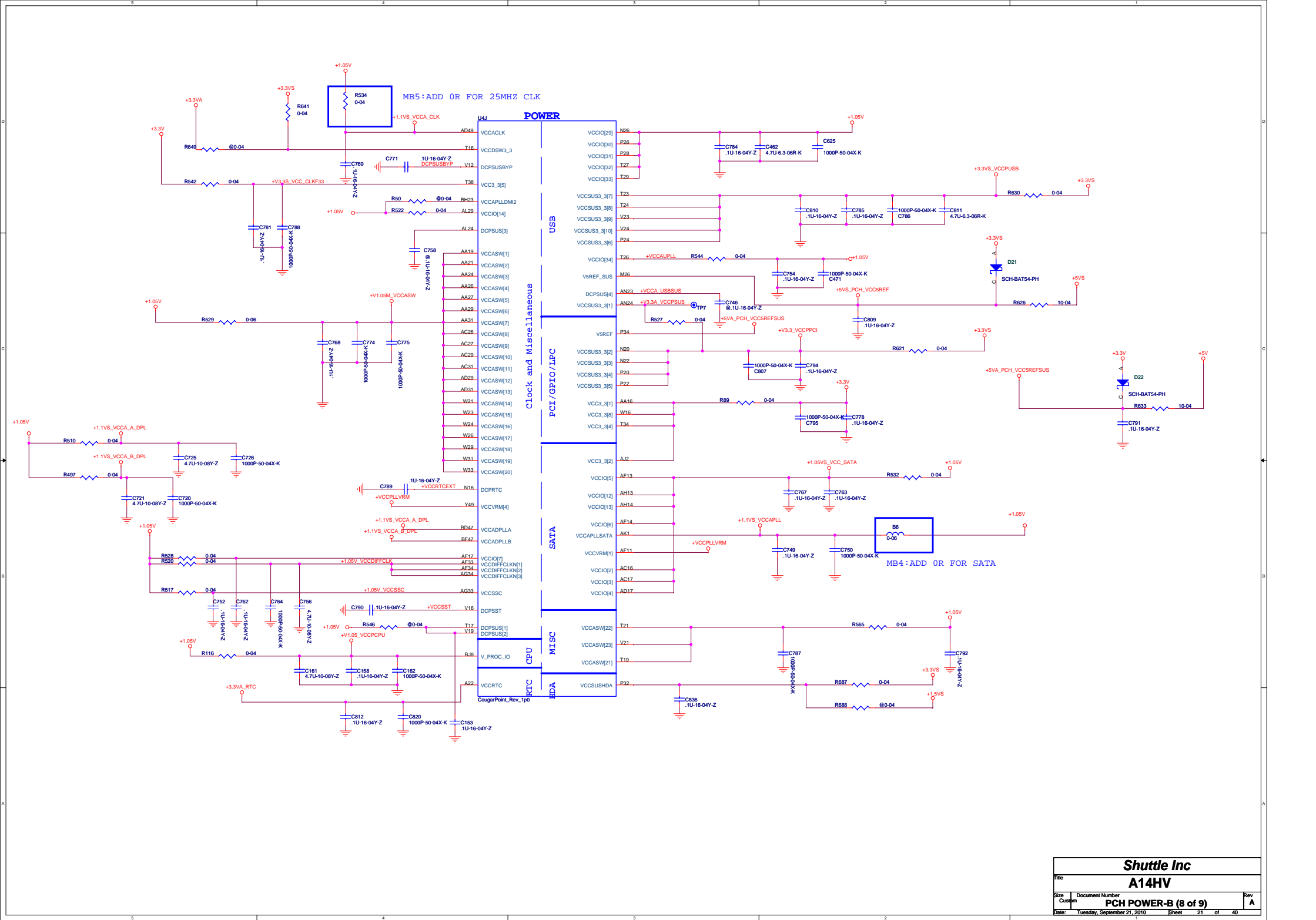
CHECK HDMI SPEC AND CRB

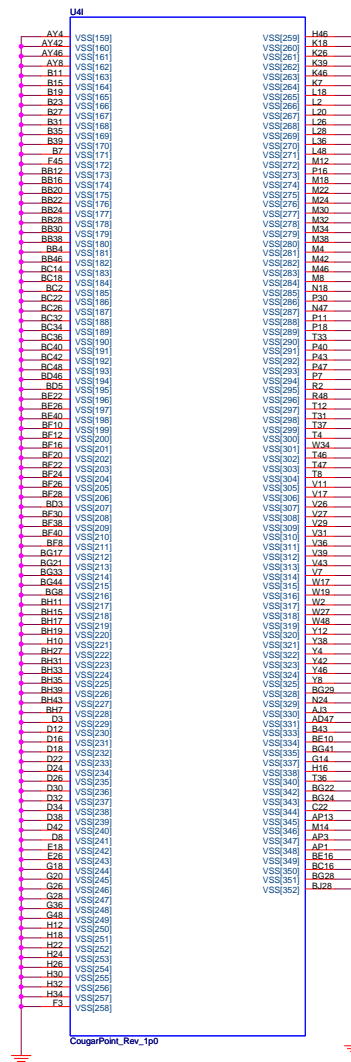
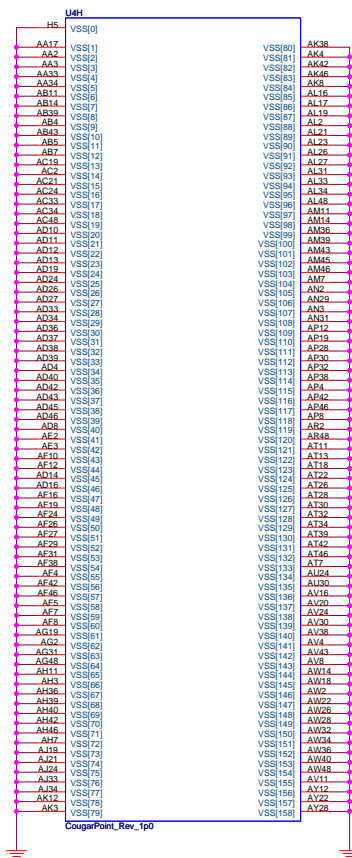


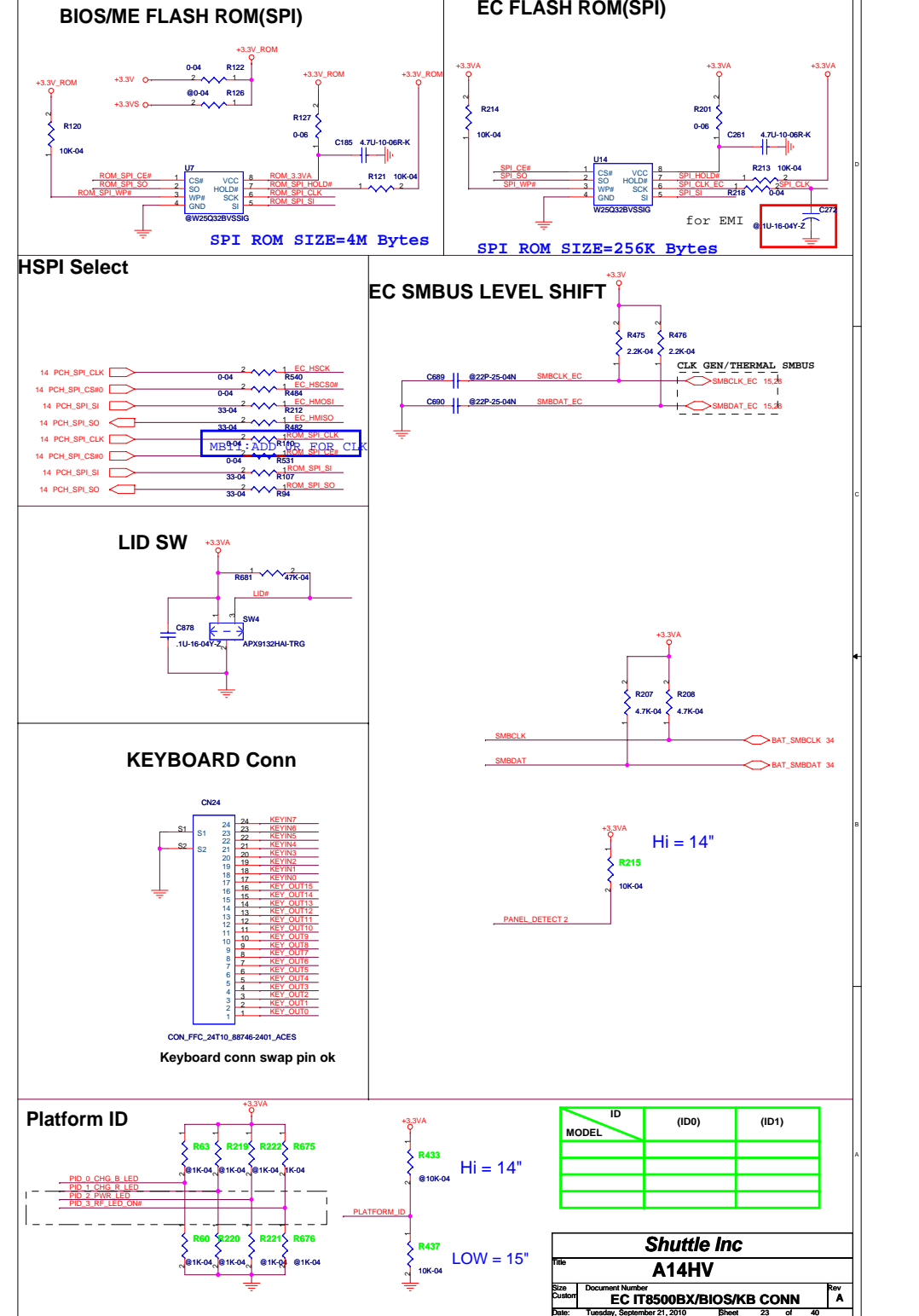
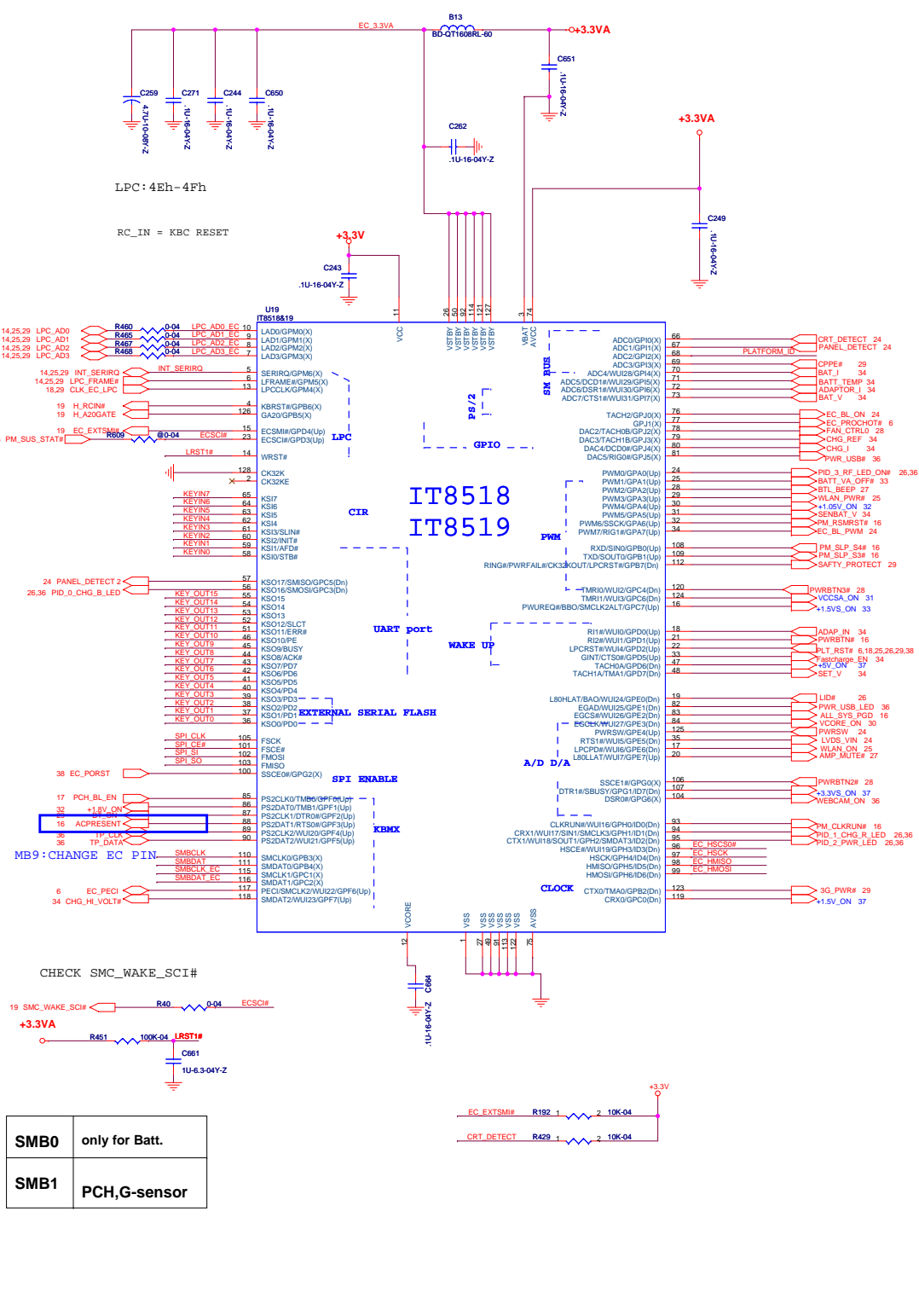












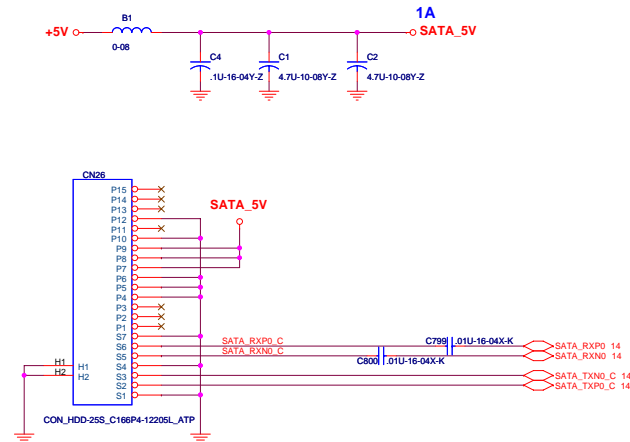
SMB0	only for Batt.
SMB1	PCH,G-sensor

ID	(ID0)	(ID1)
MODEL		

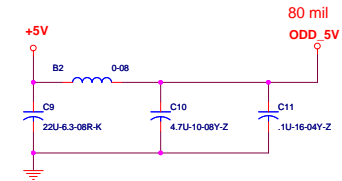
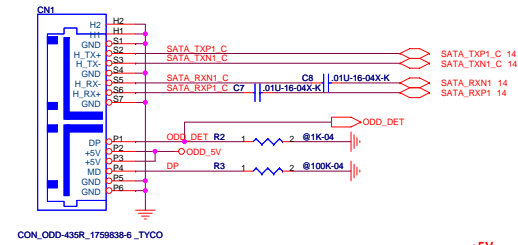




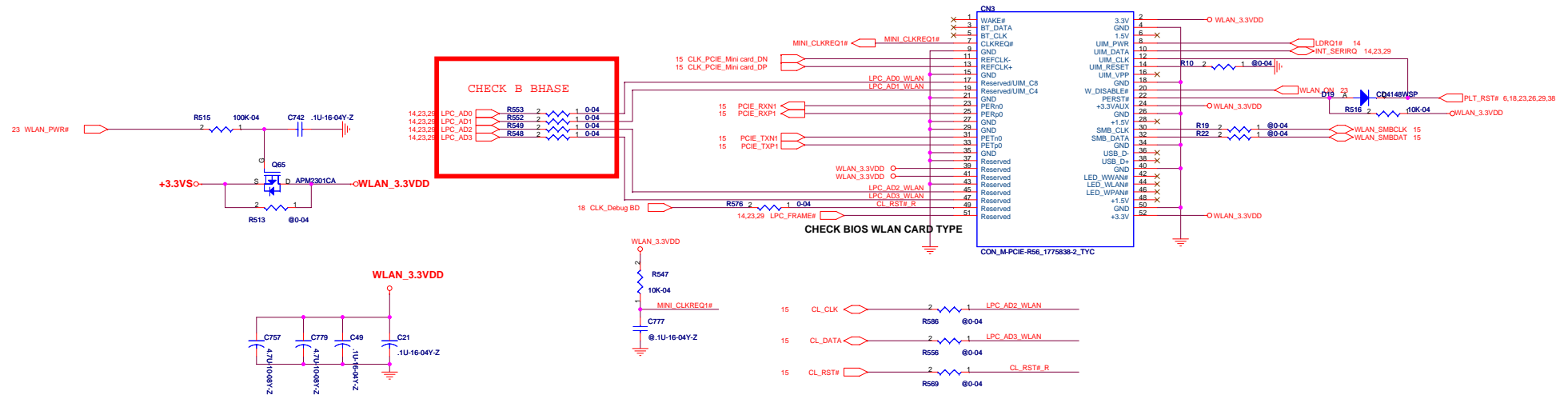
## SATA-HDD

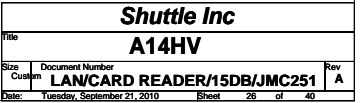


## CD-ROM



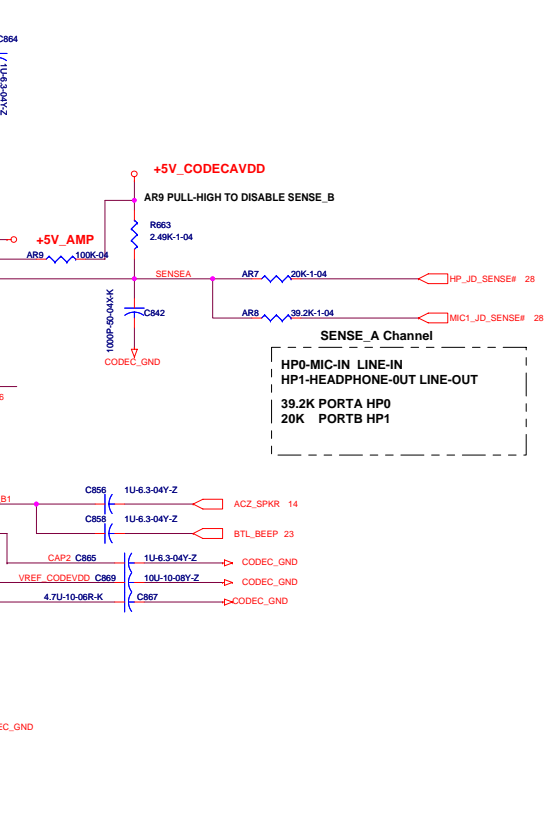
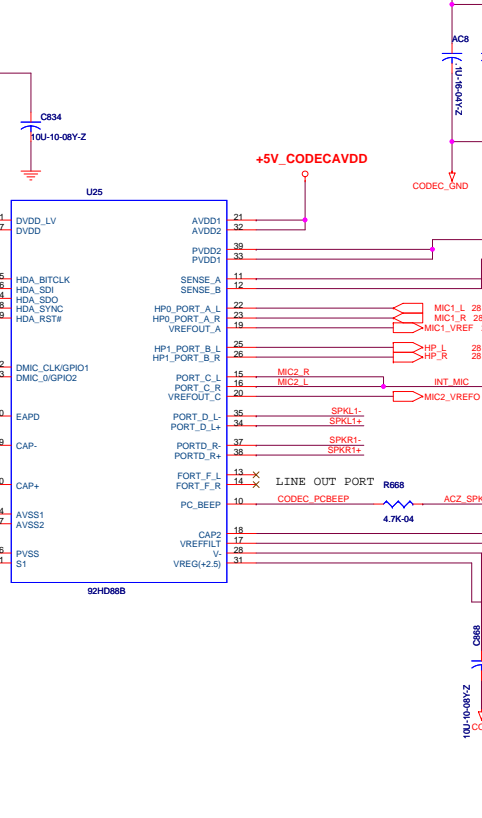
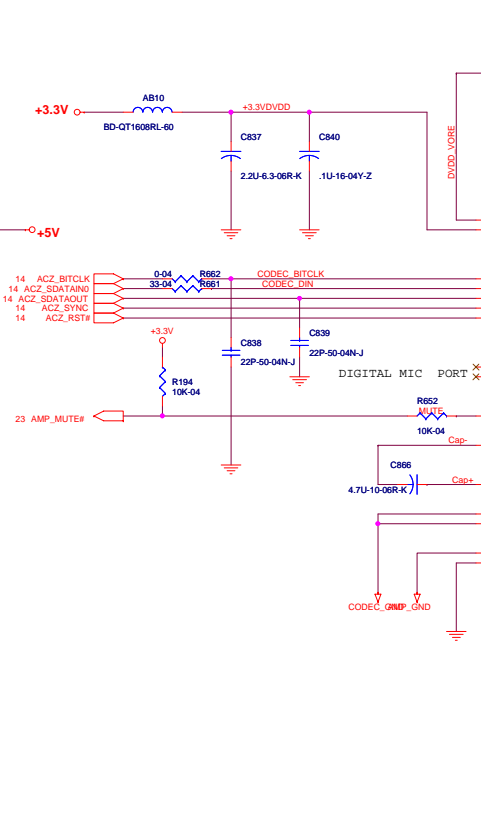
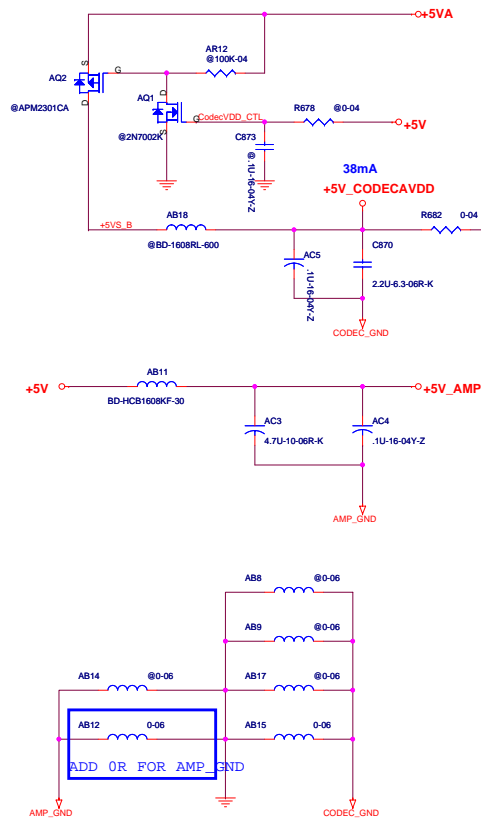
## MINI CARD CONN



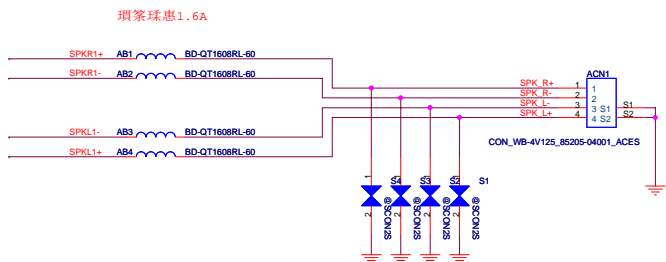


# CODEC 92HD81

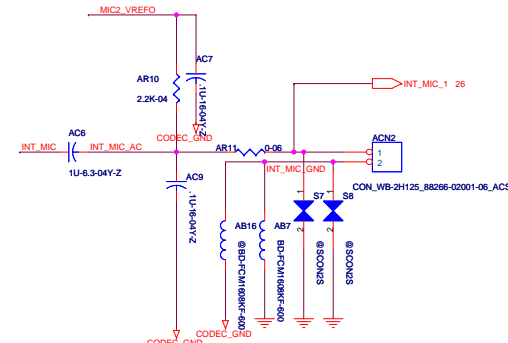
## AMP VDD



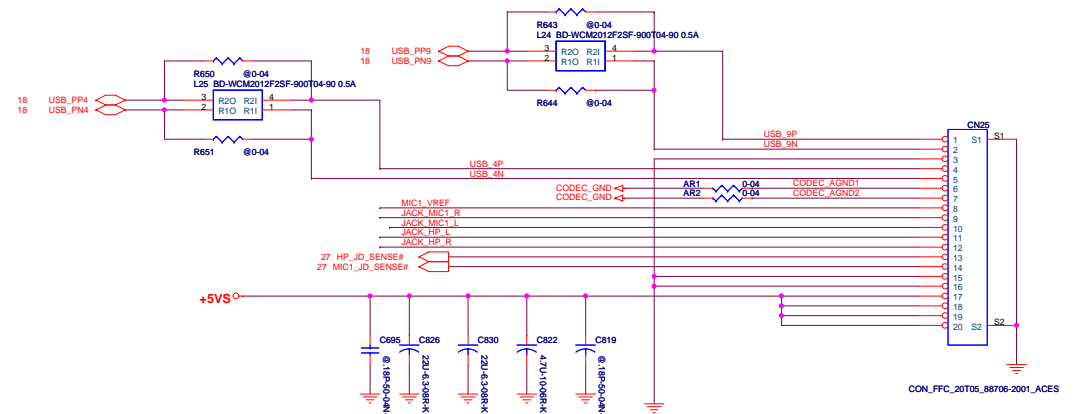
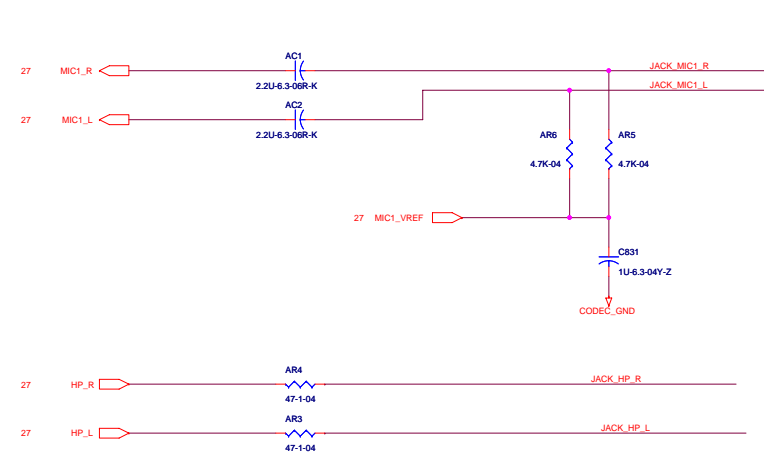
## INT\_SPEAKER



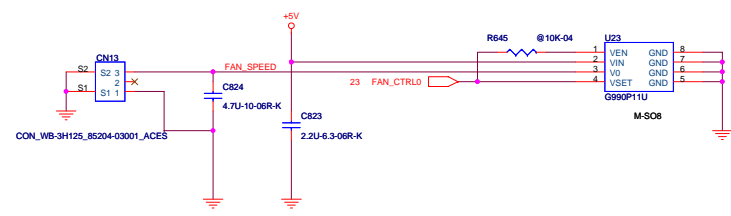
## INT\_MIC



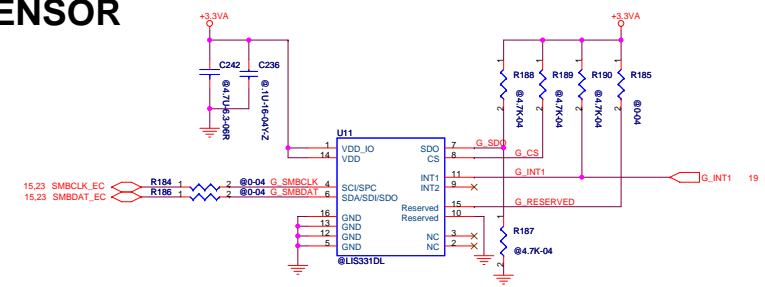
EXT MIC/EXT Line In/ EXT USB JACK



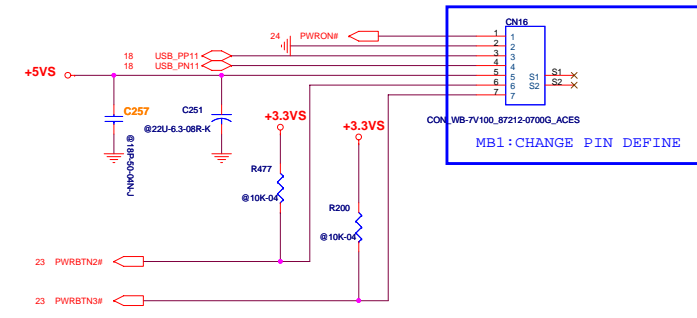
FAN CONTROLLER



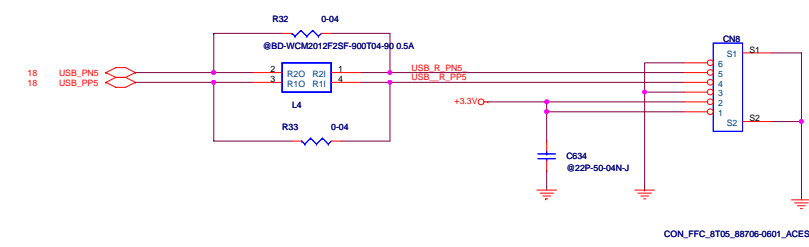
G-SENSOR



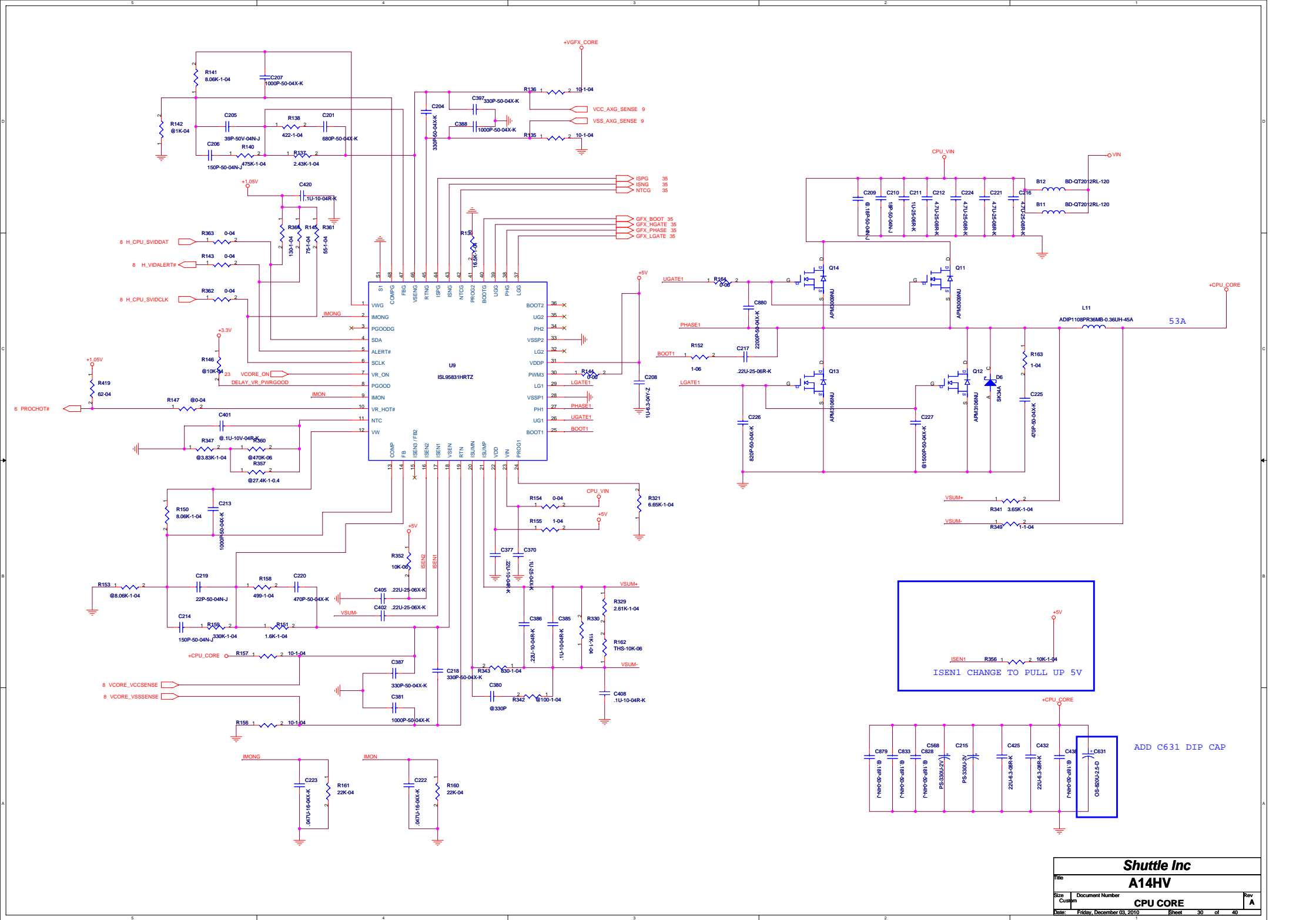
EXT USB PORT 4



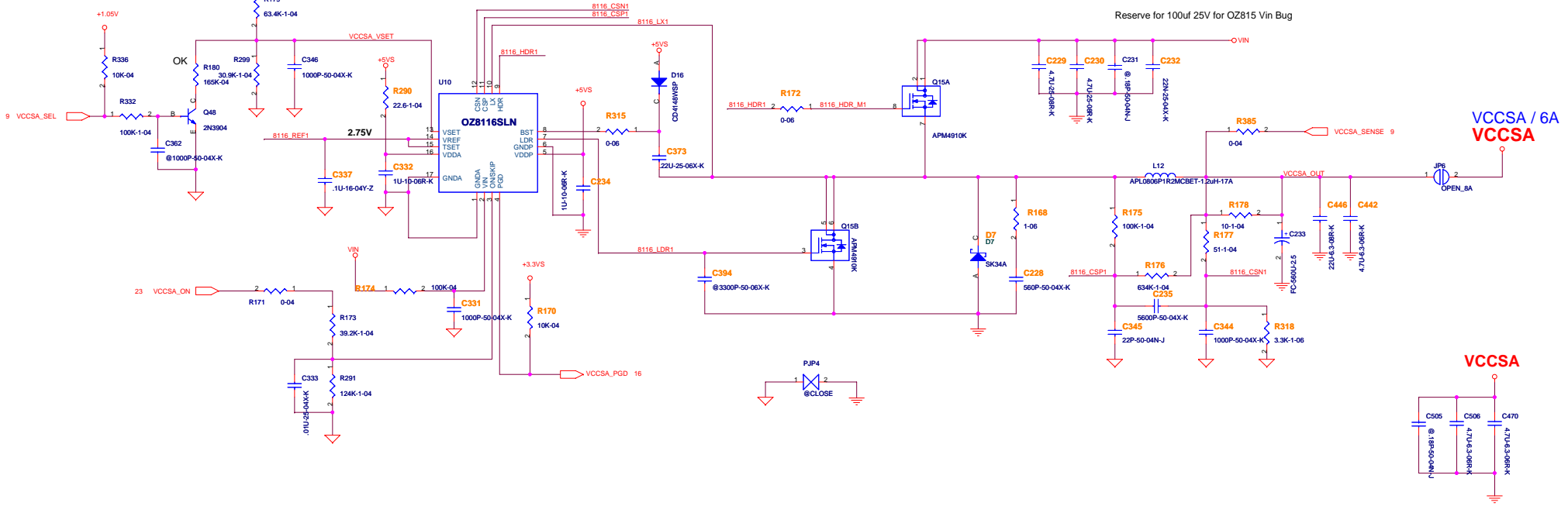
FingerPrint

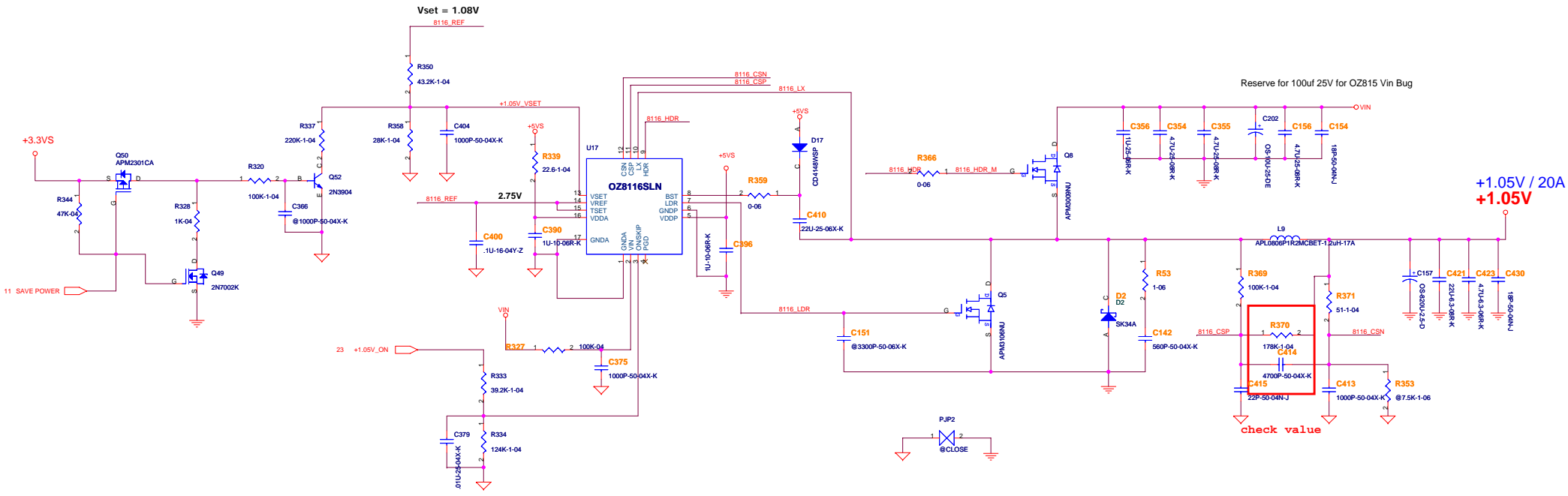




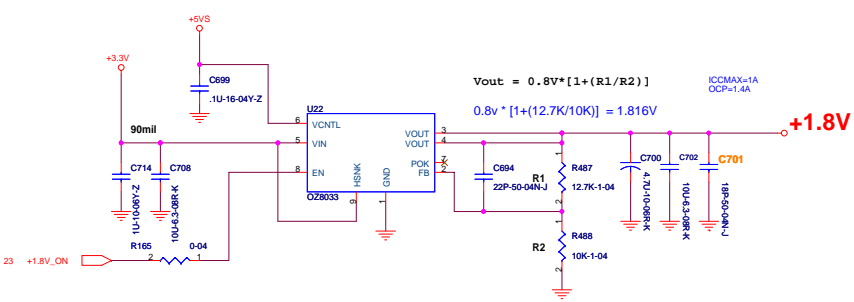
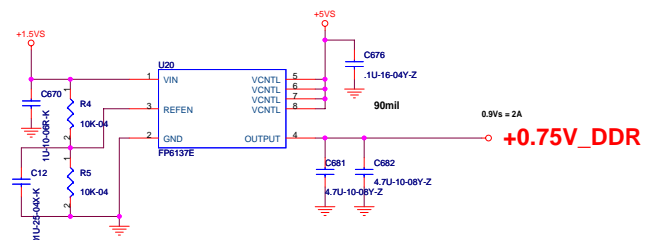


VCCSA\_SEL  
0=0.9V  
1=0.8V





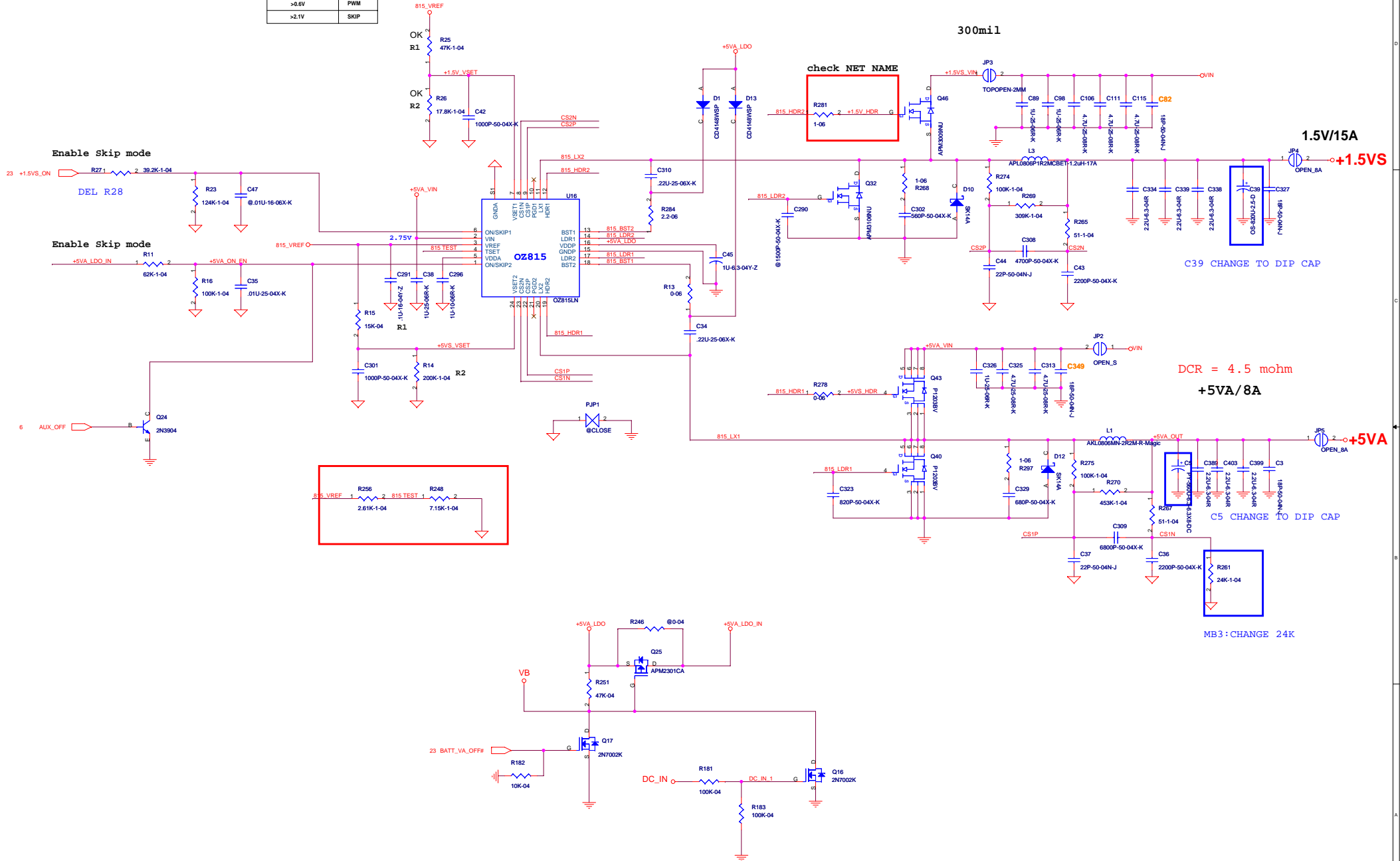
### DDR3 Termination Power



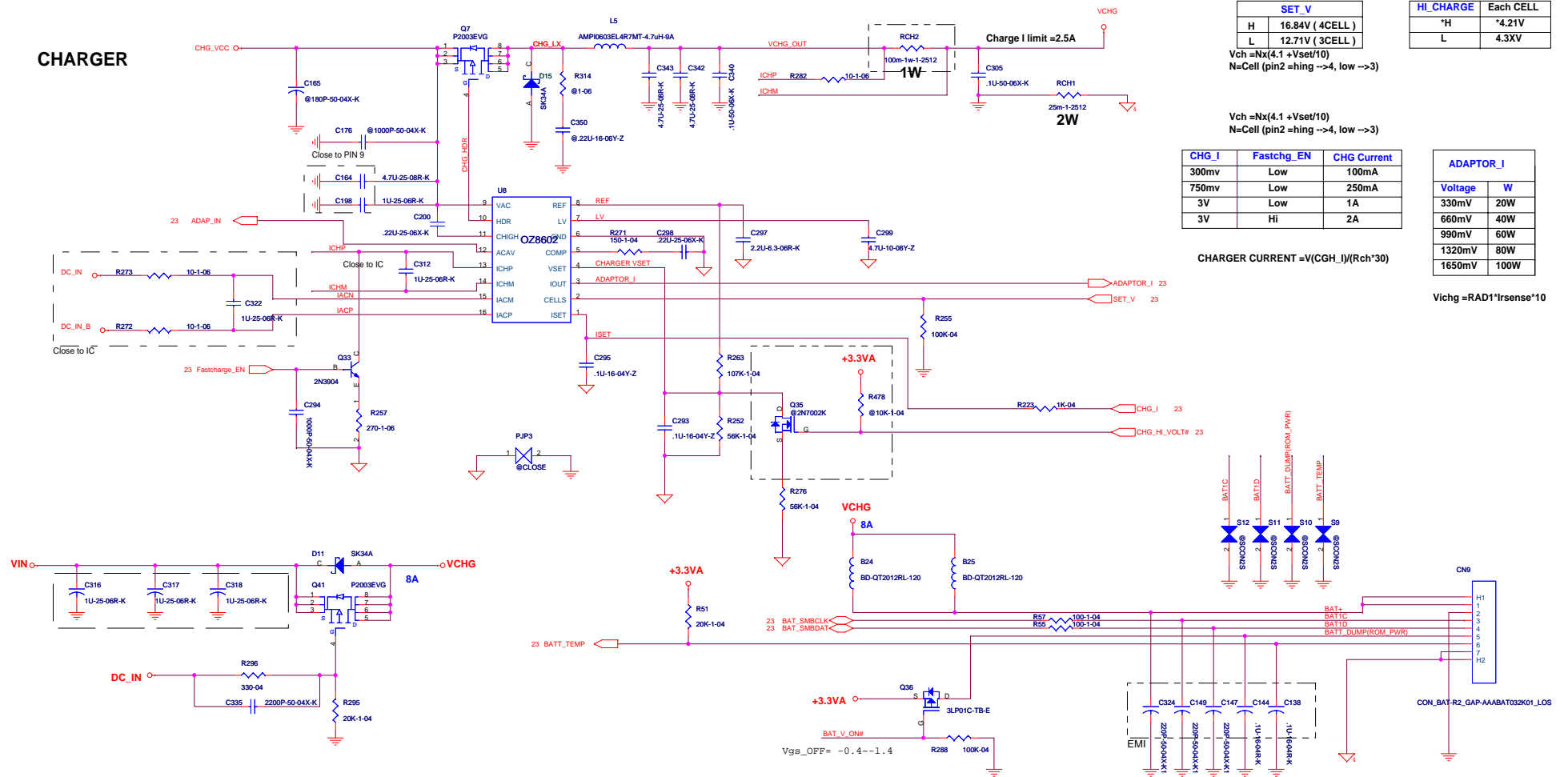


+1.8V/+5V_ON Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

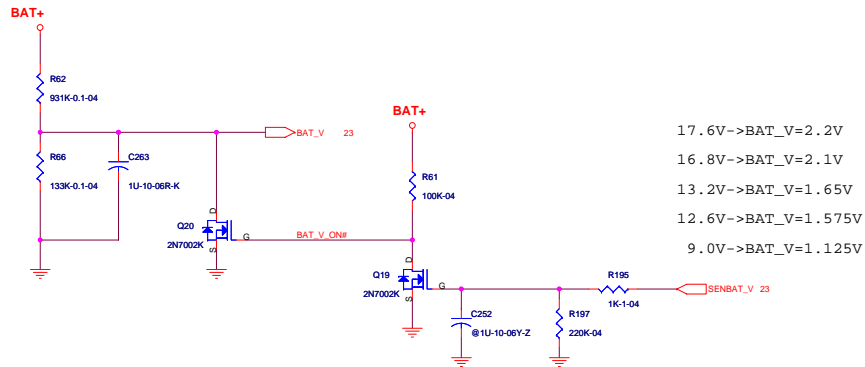
$$\text{Output Voltage} = \left[ \frac{V_{\text{ref}} \times R2}{R1 + R2} \right] \times 2$$



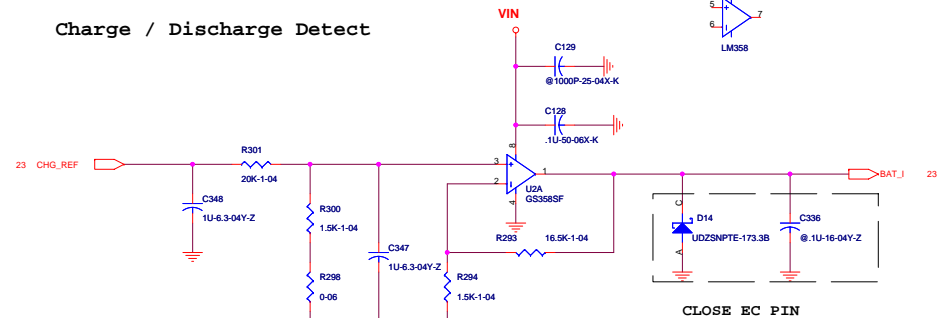
## CHARGER



## Battery Voltage Detect

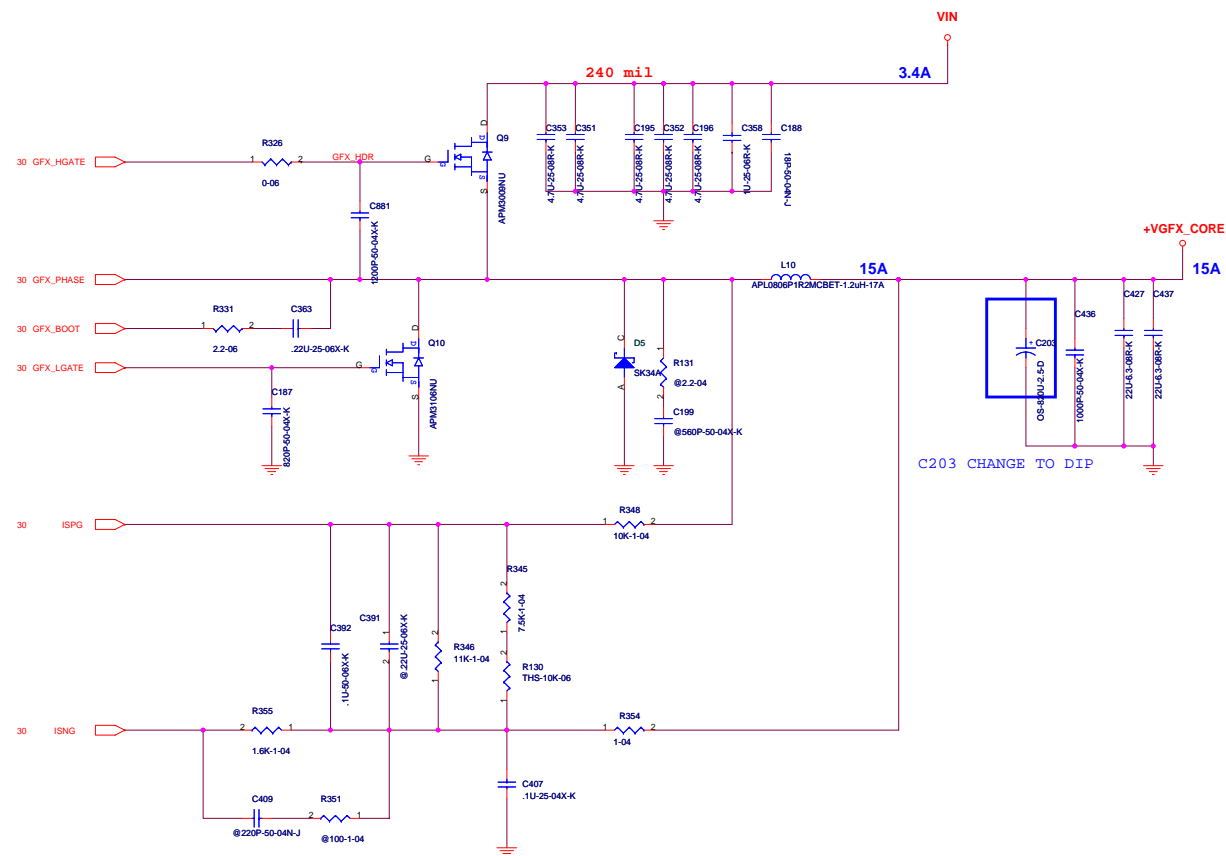


## Charge / Discharge Detect

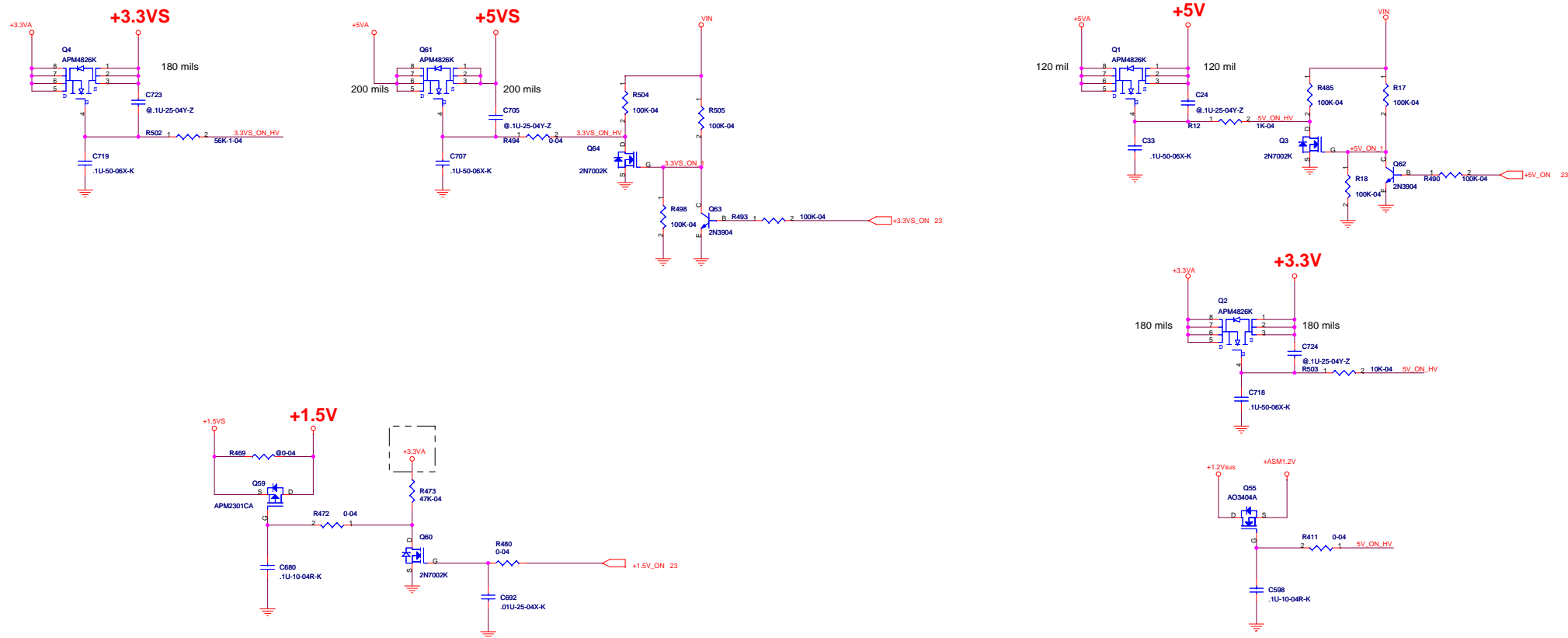


**Shuttle Inc**  
**A14HV**

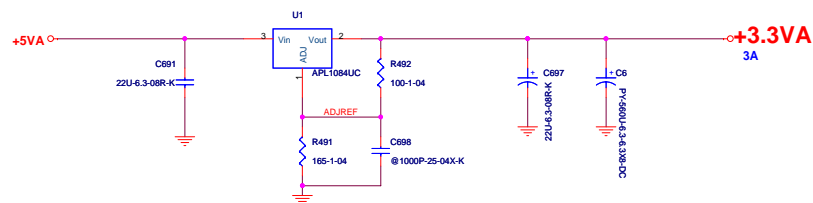
Size: Custom  
 Document Number: **BATT INCHARGER(OZ8602)**  
 Date: Tuesday, September 21, 2010  
 Sheet: 34 of 40  
 Rev: A



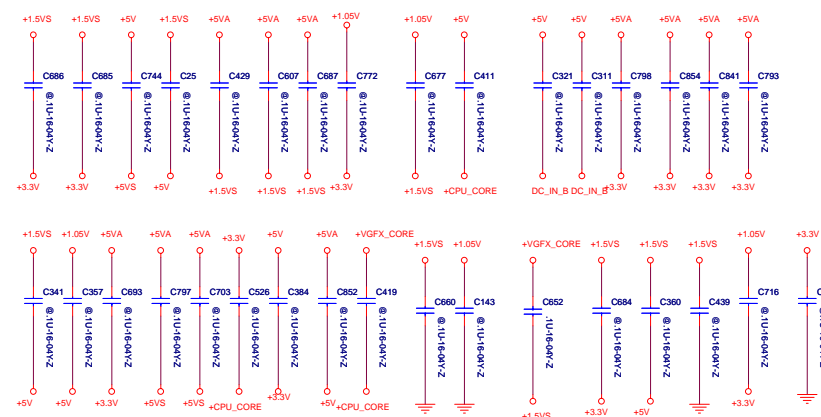


**VCCSW**

## LDO

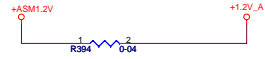
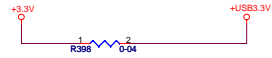


## HIGH-SPEED CAP



<b>Shuttle Inc</b>			
Title <b>A14HV</b>			
Size Custom	Document Number <b>VCC SW/+3.3VA/HIGH-SPEED CAP</b>		Rev A
Date:	Tuesday, December 07, 2010	Sheet 37 of 40	

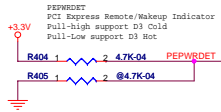
# USB3.0



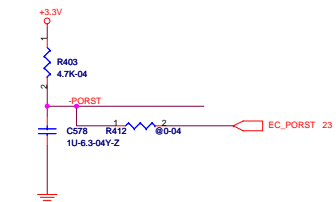
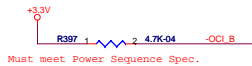
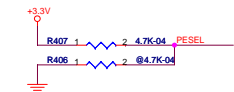
GP100	GP101	GP102	Function
1	1	0	Synchronous Mode
1	1	1	Asynchronous Mode (default)
0	0	x	Debug/Test Mode

\* GP100 GP101 GP102 internal Pull-high

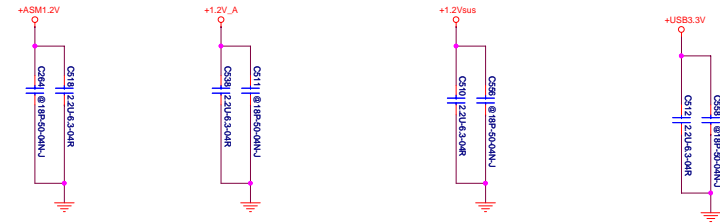
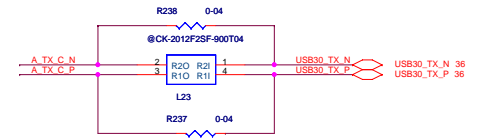
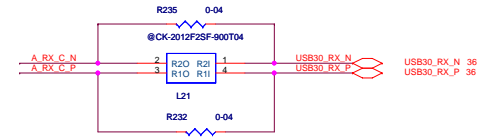
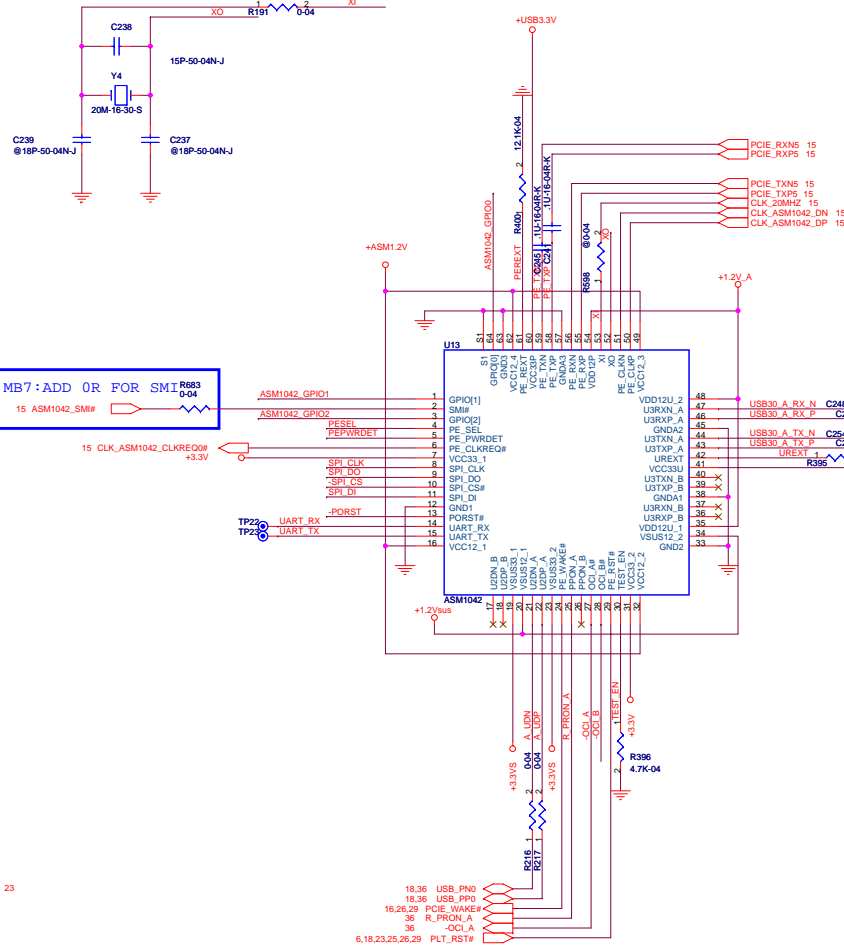
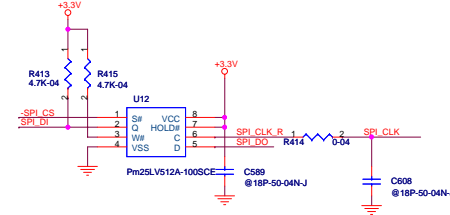
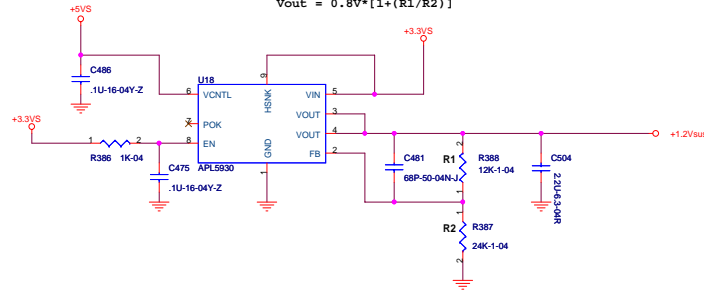
ASM1042	USB3.0	USB3.0
Clock Source	USB3.0	USB3.0
Sync	48MHz	100MHz from PCIe CLK
Async	20MHz X'tal	20MHz X'tal (For PCIe over clock)

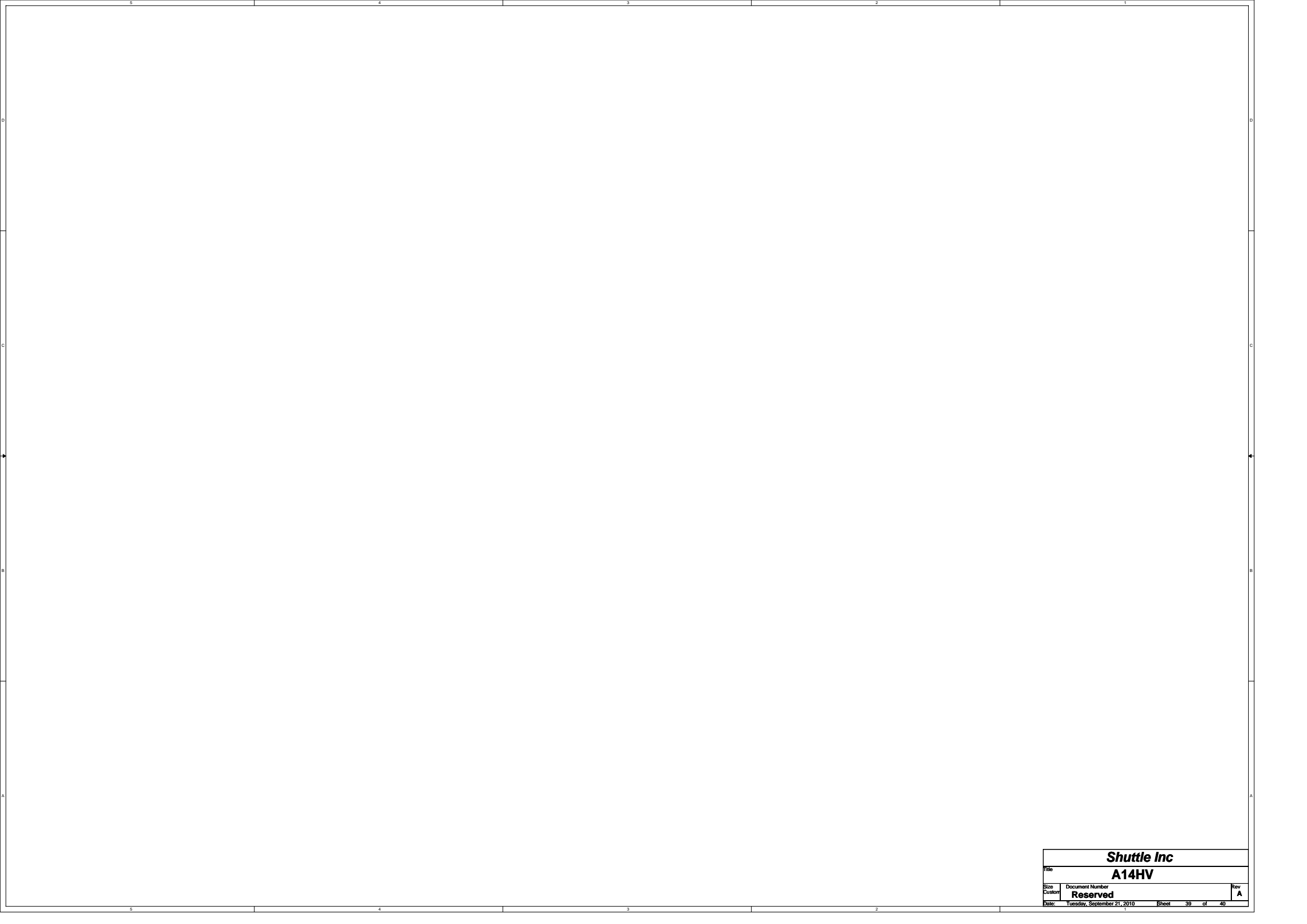


PESEL  
Pull-high for others application  
Pull-Low for Express Card/Mini card application

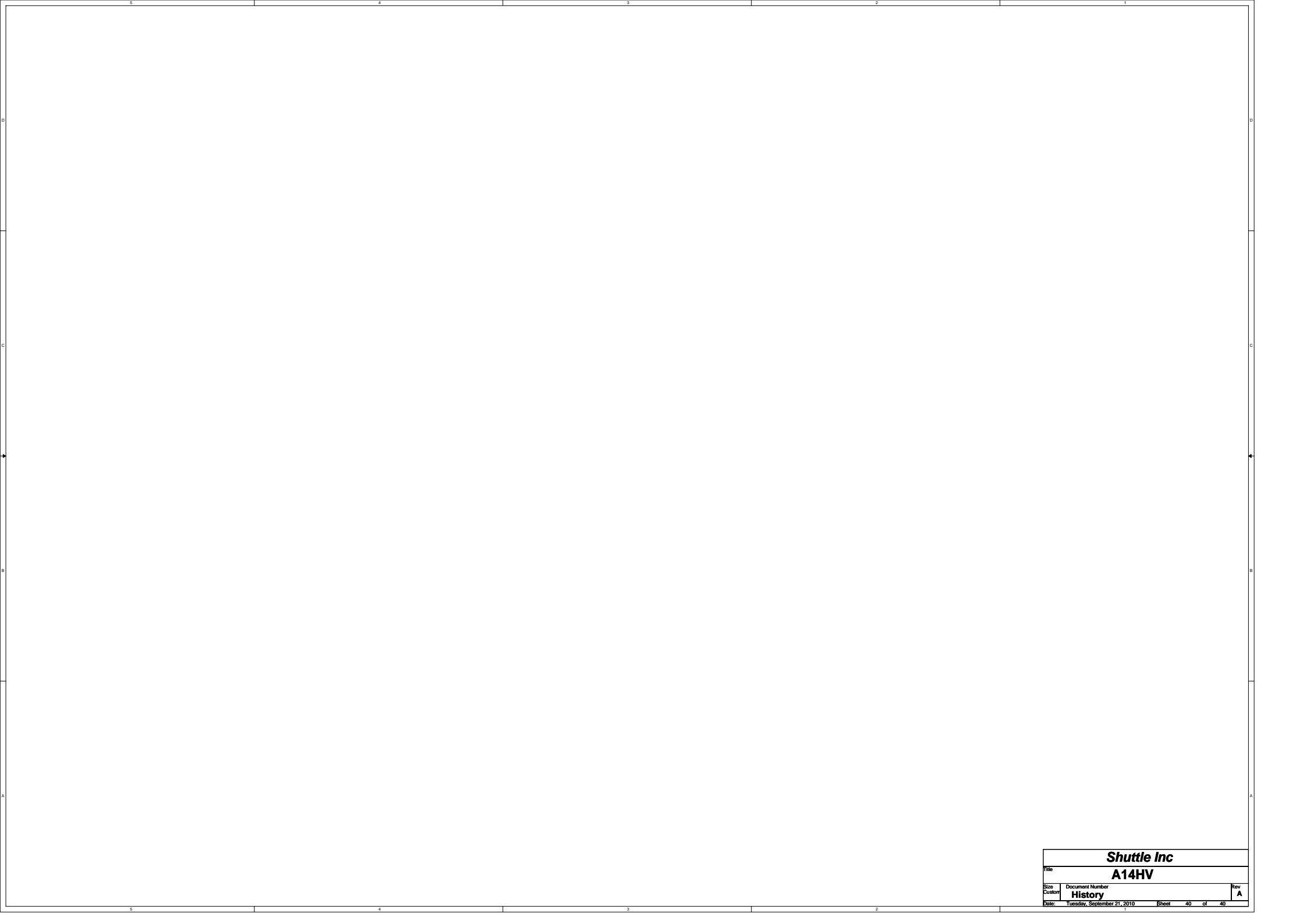


$$V_{out} = 0.8V \cdot [1 + (R1/R2)]$$





Shuttle Inc			
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Title			
Size	Document Number		
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Shuttle Inc			
A14HV			
Title			
Size	Document Number		
Custom	History		
Date	Tuesday, September 21, 2010	Sheet	40 of 40
			1